

**TO:** A. vonHalle  
**FROM:** P. Sichta

**SUBJECT:** Closeout note for Timing and Synchronization, Job 5401

**Date: July 23, 2008**

**Scope**

*The Facility Timing and Synchronization System (T&S) will provide the hardware and software that facilitates the synchronization of hardware and equipment to the 'microsecond' degree, and computer programs on NCSX computers to the 'seconds' degree.*

**Status**

- *This job has completed the CDR phase, but awaits a PDR based upon the approved workscope.*

**Interfaces**

*WBS54 will ultimately interface with most NCSX diagnostics and engineering subsystems. For MIE it will be limited to a few, depending upon the approved workscope.*

**Specifications**

*An SDD and Data Dictionary have been completed and are on the NCSX website.*

**Schematics and PIDs**

*none.*

**Models**

*none.*

**Drawings**

*none.*

**Analyses**

*none.*

**Testing**

*none.*

**Costs**

*Costs are posted on the NCSX website.*

**Remaining Work**

- PDR, FDR, Installation and test.

**Lessons Learned:**

*none.*

**Conclusion:**

*Upon job resumption, review current technologies and proceed to PDR.*

# Central Controls and Computing

## WBS53-57

P. Sichta

*WBS5 Work Package Manager*

# Agenda



- Introduction
- Requirements and Interfaces
- Cost and schedule
- Risks and mitigation
- Responses to past review recommendations

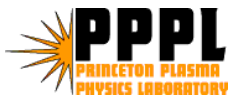
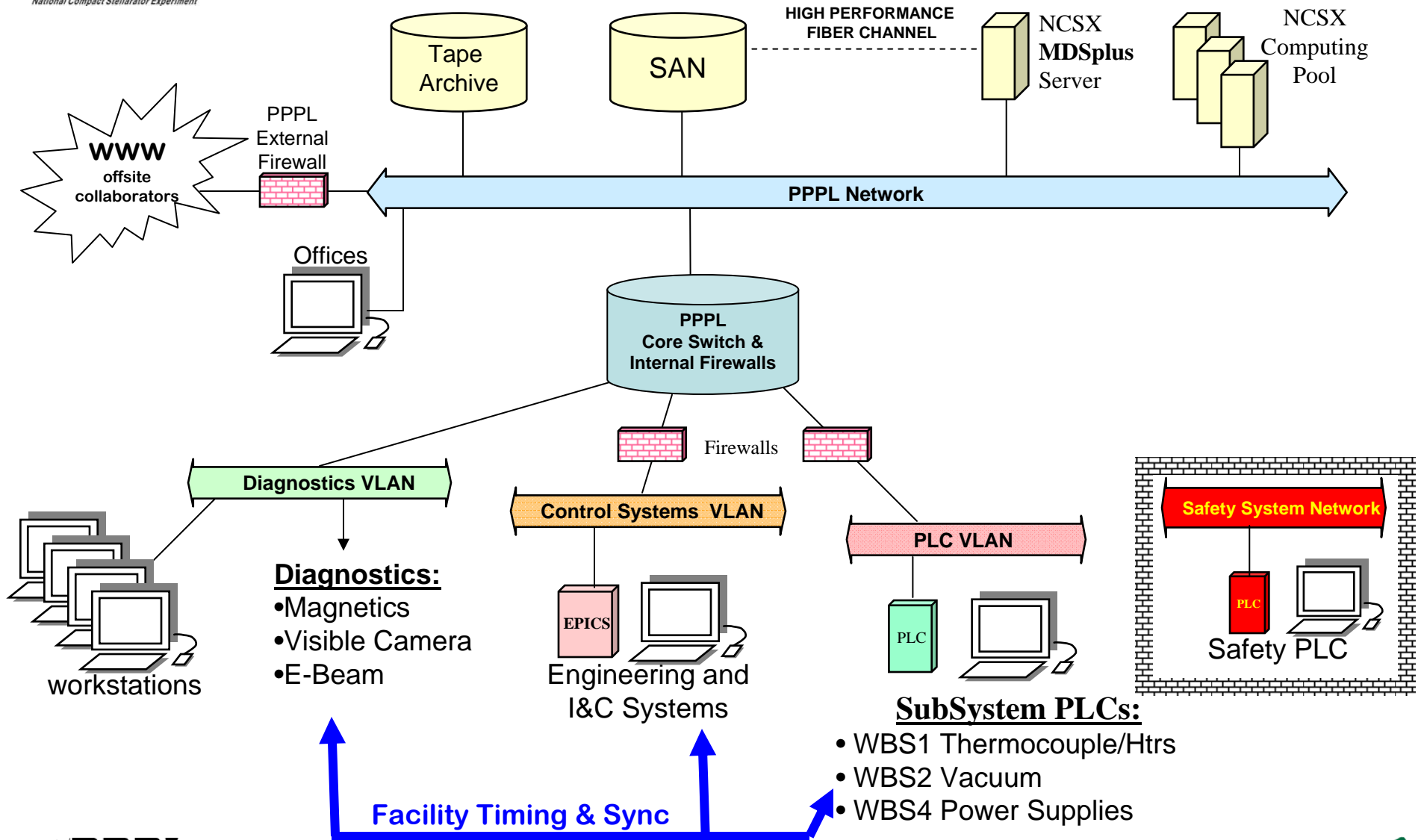
# Introduction



Central Controls and Computing will provide the equipment and services to support: 1) integrated and remote control; 2) data acquisition, analysis, and storage; 3) facility timing and synchronization; 4) central safety and interlocks.

- **Network and Fiber Optic Infrastructure (WBS 51)**
- **Central Instrumentation and Control (WBS 52)**
- **Data Acquisition and Facility Computing (WBS 53)**
- **Facility Timing and Synchronization (WBS 54)**
- **Real-Time Plasma and Power Supply Control (WBS 55)**
- **Central Safety and Interlock System (WBS 56)**
- **Management and Integration (WBS 58)**

# NCSX Computing Overview



SC Project Review of NCSX, April 8-10, 2008

P. Sichta - page 4



# Requirements



- An *NCSX System Design Description* (SDD) was written in 2003, before CD-2. The primary elements of that design remain intact.
- My current estimate is derived from the SDD, ongoing technical discussions and design reviews, and recent experience with similar systems on NSTX.
- A **WBS5 System Requirements Document** (SRD, BSPEC) will be reviewed and approved prior to the *Preliminary Design Review* for each WBS5 element.
- Design Complexity & Maturity
  - Many of the technologies for WBS5/NCSX are currently in use on NSTX, so complexity is low for our experienced staff.
  - The *current workscope* has completed neither **Preliminary** nor **Final design**, so the maturity is medium.

# CD-4 Interface List



WBS51 Network & Fiber Optic	WBS1 Thermocouple/Heater Local I&C WBS2 Vacuum/Fueling Systems WBS3 Diagnostics WBS4 Power Systems
WBS52 Central I&C	WBS1 Thermocouple/Heater Local I&C WBS2 Vacuum/Fueling Systems WBS4 Power Systems
WBS53 Data Acquisition and Management	WBS1 Thermocouple Local I&C WBS2 Vacuum/Fueling Systems WBS3 Diagnostics WBS4 Power Systems
WBS54 Timing & Synchronization	WBS3 Diagnostics WBS4 Power Systems
WBS55 Real-Time Control	WBS2 Vacuum/Fueling Systems WBS4 Power Supply Control
WBS56 Central Safety and Interlocks	<b>Access Control:</b> WBS4 Power System Areas, WBS7 Test Cell. <b>SubSystem Interlocks:</b> WBS4 Power Systems. <b>NCSX (Global) E-Stop.</b>

# Basis of Estimate



- Labor:
  - referenced actual engineering hours from FY97-99 for the NSTX first plasma.
  - experience with similar activities for NSTX.
  - ‘expert’ estimates (e.g. Erik Perry).
- M&S
  - recent purchase of parts for NSTX and other lab infrastructure projects.
  - catalog prices.
  - includes spares and service contracts.
  - selective use of NSTX equipment.



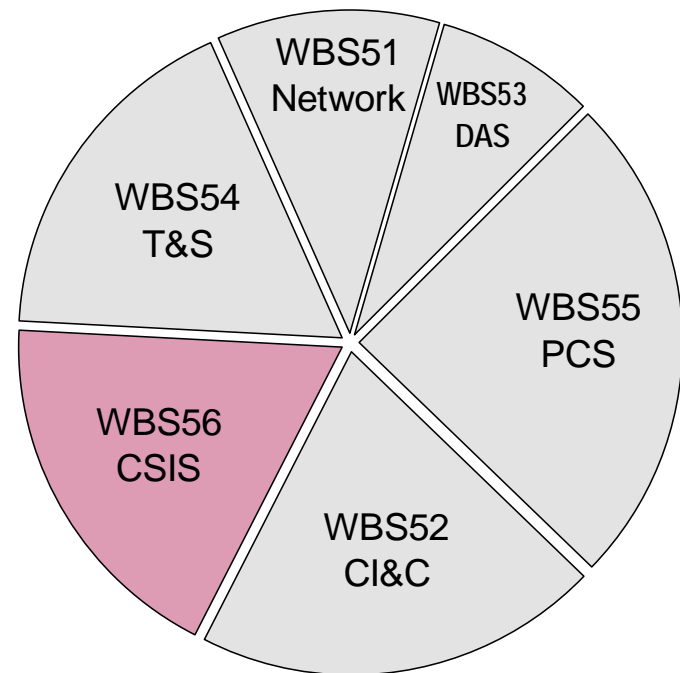
# WBS5 Aggregate Cost

Reference *WAFs* for labor and M&S detail for WBS51-58.

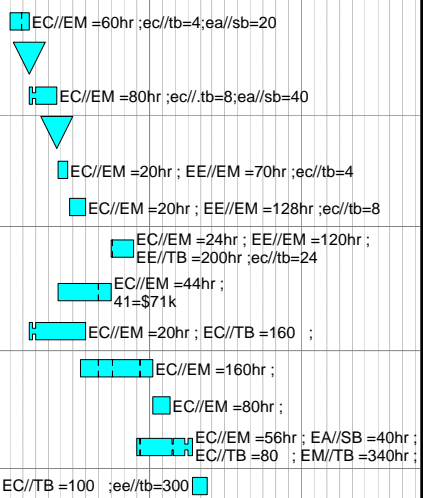
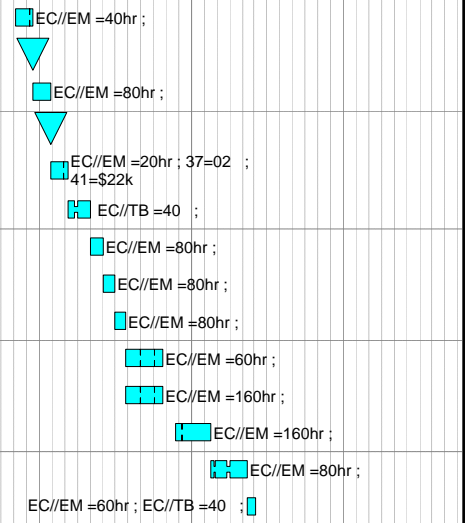
[http://ncsx.pppl.gov/Rebaseline/Rebaseline\\_index.htm](http://ncsx.pppl.gov/Rebaseline/Rebaseline_index.htm)

WBS5 ETC = \$ 2.1 M

Softwr/Elec Engineering: **3.6 years**  
Elec/Mech/Draft Tech: **3.1 years**  
'Materials & Services': **\$ 432 K**



Activity ID	MILE-STONE LEVEL	Activity Description	Duration (work days)	SHIFTS	Forecast Start	Forecast Finish	Total Float	Cost to Complete	FY				
									FY08	FY09	FY10	FY11	FY12
<b>53 - Data Acquisition &amp; Facility Computing</b>													
<b>Job: 5301 - Data Acquisition-SICHTA</b>													
R53-10		Preliminary Design	30		03AUG09*	14SEP09	182	5,591.20					
R53-11		PDR	0			14SEP09	182	0.00					
R53-20		Final Design	30		15SEP09	26OCT09	182	11,378.72					
R53-21		FDR	0			26OCT09	182	0.00					
R53-30		Procurement	30		27OCT09	09DEC09	182	32,291.40					
R53-40		Installation	30		10DEC09	01FEB10	182	3,006.00					
R53-50		MDSplus Installation	20		02FEB10	01MAR10	182	11,509.60					
R53-60		MDSplus Programming - Tree Design	20		02MAR10	29MAR10	182	11,509.60					
R53-70		MDSplus Programming - Shot Sync	20		30MAR10	26APR10	182	11,509.60					
R53-100		Applications Support (3 Diags)	60		27APR10	21JUL10	182	8,632.20					
R53-110		Programming - Misc.	60		27APR10	21JUL10	182	23,019.20					
R53-80		MDSplus Programming - Dispatcher	60		23AUG10*	15NOV10	160	23,641.28					
R53-90		MDSplus Programming - Acquisition	55		16NOV10	10FEB11	160	12,092.80					
R53-120		Test	14		11FEB11	02MAR11	160	12,227.60					
<b>54 - Facility Timing &amp; Synchronization</b>													
<b>Job: 5401 - Facility Timing &amp; Synchron.-SICHTA</b>													
R54-10		Preliminary System Design	30		02NOV09*	15DEC09	202	11,403.80					
R54-11		PDR	0			15DEC09	202	0.00					
R54-20		Final SystemDesign	40		16DEC09	19FEB10	202	17,052.80					
R54-21		FDR	0			19FEB10	302	0.00					
R54-30		Preliminary Design - Clock Dist.	20		22FEB10	19MAR10	302	15,311.10					
R54-40		Final Design - Clock Dist.	30		22MAR10	30APR10	302	25,664.84					
R54-50		Test - Clock Dist.	40		29JUN10	24AUG10	262	42,142.08					
R54-60		Procurement	90		22FEB10*	28JUN10	212	101,257.28					
R54-70		UNT - Timing & Seq Emulation (FPGA Pgm)	90		16DEC09*	30APR10	342	14,901.40					
R54-80		UNT - Device Driver Prog (EPICS/MDSplus)	120		19APR10	06OCT10	202	23,058.08					
R54-90		Central Clock (EPICS) Programming	30		07OCT10	17NOV10	202	12,092.80					
R54-100		Installation	90		30AUG10*	13JAN11	169	50,074.31					
R54-110		Test	25		14JAN11	17FEB11	169	45,340.80					

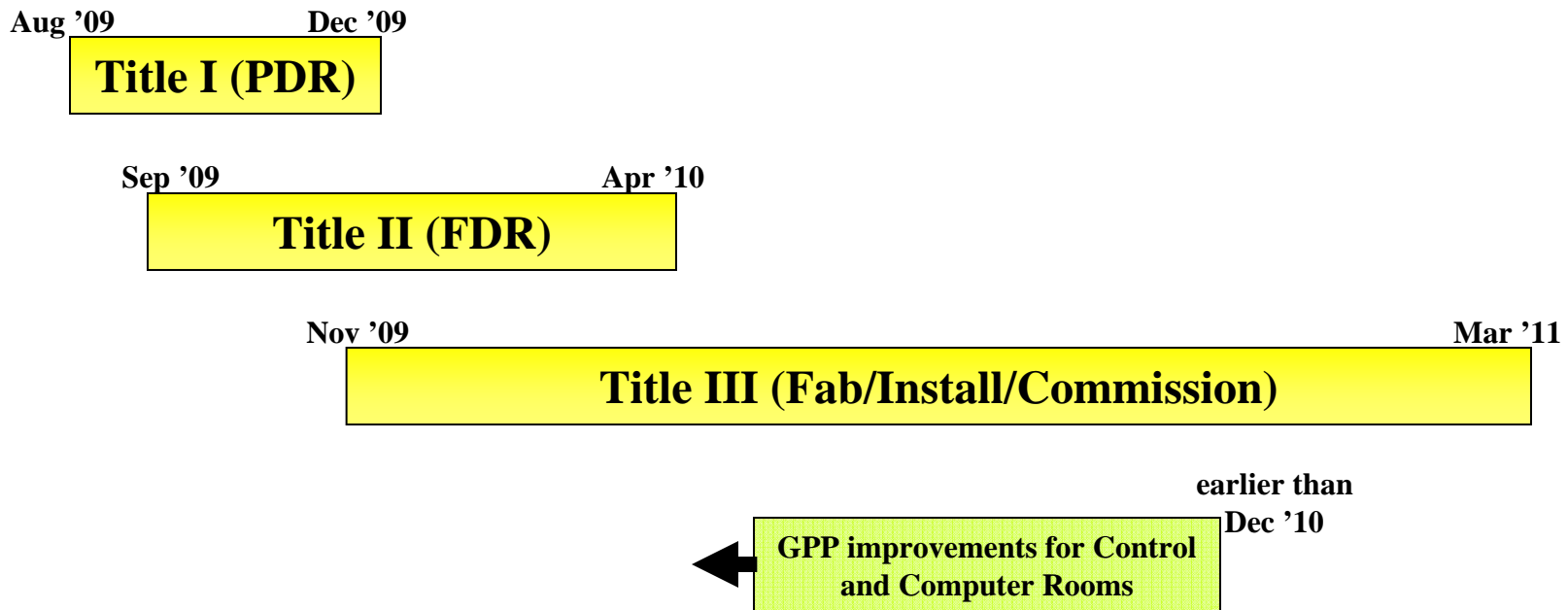


# WBS51–WBS56 Aggregate Schedule



Reference *Resource Loaded Schedule* pages 53-56  
for schedule detail for WBS51 – WBS58.

[http://ncsx.pppl.gov/Reviews/FY08/BCP\\_2008/Docs/NCSX\\_RLS0403.pdf](http://ncsx.pppl.gov/Reviews/FY08/BCP_2008/Docs/NCSX_RLS0403.pdf)



# Risks and Mitigation



Reference *NCSX Risk Register* (page 2, item 'e') for WBS5 risks.

[http://ncsx.pppl.gov/Reviews/FY08/BCP\\_2008/Docs/RR\\_Rev28a.pdf](http://ncsx.pppl.gov/Reviews/FY08/BCP_2008/Docs/RR_Rev28a.pdf)

Risk Description	Mitigation Plan	Likelihood	Consequence	Risk Ranking
Loss of staff with experience in specialized software will delay availability of Central I&C system.	Staff have recently been brought on board in anticipation of growing NCSX I&C needs. The planned shutdown of NSTX after FY10 will increase the availability of similar resources for NCSX.	VU	Marginal	Low

# Response to Past Review Findings



## 1. Work with ES&H on Safety System Requirements and design basis.

- PPPL's *ES&H Directives Manual, section 2-5 "Personnel and Safety Interlock Systems"* is in the process of being updated.

## 2. Document Basis of Estimate

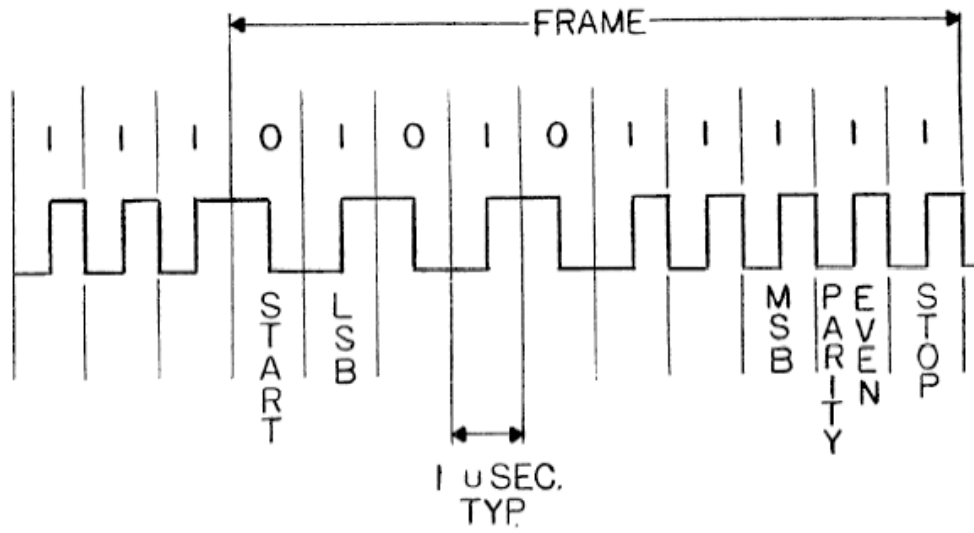
- A WBS5 notebook has been prepared to compile the design basis.
  - Copies of recent requisitions for similar equipment.
  - Catalog cut-sheets with prices.
  - Actual NSTX engineering-hours (labor) tabulation for first plasma.

# Conclusion



The NCSX central controls and computing are **similar in both function and scale to NSTX**. The availability of a technically diverse and **experienced staff** provides confidence that the WBS5 work elements will effectively support the NCSX project's CD-4 objectives.

PPPL Clock Link Timing Waveform  
20October2003



# INCAA DIO2 Timing Highway Waveform

2003-09-12

Signal. which, because it is bi-phase encoded, results in a clock of 1MHz when no data is received. A rising edge within the middle of a 1µs period represents a logical '0' and a falling edge a logical '1'. During idle state a logical '1' is bi-phase encoded. When data is received this will be a timing event which can be used as a trigger of the timing channels. The received event can also be recorded in a 32 events deep FIFO including a time stamp.

The DIO2 is also capable of encoding and transmitting timing highway events. A software command or a selected trigger can cause the transmission of a timing event.

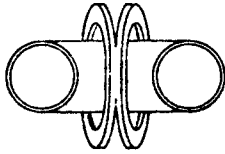
The encoded timing highway signal starts with a start bit (logical '0'), followed by 7 data bits (LSB first), a even parity bit and a stop bit (logical '1'). Because 1 bit lasts 1µs the transmission of a timing event takes 10µs.

An example of the timing highway signal can be seen below.

The diagram shows a timing event of 10µs duration. The signal is represented as a square wave where 'Light' is high and 'Dark' is low. The bits are: 1 (high), 1 (high), 1 (high), 0 (low), 1 (high), 1 (high), 0 (low), 1 (high), 0 (low), 0 (low), 0 (low), 1 (high), 1 (high), 1 (high), 1 (high). The bits are grouped as: Start bit (0), 7 data bits (LSB to MSB: 1, 1, 1, 0, 1, 1, 0), Even parity (1), and Stop bit (1).

The 1MHz clock which is encoded in the signal at all times is decoded out of the timing highway signal and can be used (multiplied by 10) to clock the timing channels with.





**CICADA  
ENGINEERING  
SPECIFICATION**

DOCUMENT NO.  
TFTR-10B4-H401

PAGE 1 OF 17

DATE- 1/24/78

SUBJECT  
Facility Clock Subsystem

PREPARED BY  
H. Del Gatto  
H. Del Gatto

APPROVED BY

*R. S. Quinn*  
SYSTEM MANAGER

*J. J. [unclear]* 5-11-77  
PPL QUALITY CONTROL

*J. R. [unclear]*  
E/G ENGINEERING MANAGER

*R. [unclear]*  
PPL COGNIZANT PHYSICIST

*K. [unclear]*  
PPL ENGINEERING MANAGER

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**REVISIONS**

DATE	DESCRIPTION

## 1.0 Abstract

This specification, in conjunction with referenced documents, sets forth all characteristics of the subject subsystem (Facility Clock System). The intended use of this document is to provide a minimum design goal for the subsystem as well as a working document for subsequent users.

## 2.0 Reference Documents

- 2.1 IEEE Standard Modular Instrumentation and Digital Interface System (CAMAC), 1975. The Institute of Electrical and Electronic Engineers, Inc.
- 2.2 Telemetry Standards (revised January 1971) IRIG, Document NO. 106-71.
- 2.3 USA Standard Codes for Information Exchanges, USAS X3.4-1968, ANSI X3.15-1966, ANSI X3.16-1966.
- 2.4 Printed Circuit Artwork Specification, TFTR-10A2-H53.
- 2.5 Printed Circuit Board Fabrication and Assembly Specification, TFTR-10A2-H54.
- 2.6 Electronic Schematic Specification, TFTR-10A2-H55.
- 2.7 Standard Timing Signal Specification, TFTR-10A2-H57.
- 2.8 Reliability, Quality Control and Temperature Cycling Specification, TFTR-10A2-H58.

### 3.0 Introduction

The Facility Clock Subsystem (FCS) when used with appropriate decoding receivers provides the means for generating multiple timing signals throughout a distributed computerized instrumentation, control and data acquisition (CICADA) system. The FCS will be used at the Tokamak Fusion Test Reactor (TFTR) site at Princeton, for the purpose of providing a means of accomplishing synchronous control throughout the facility.

3.1 The timing signal characteristic of the system is accomplished by distributing a coded clock signal to various functional parts of the CICADA system. Remote receivers may utilize this clock to achieve real time synchronism as well as derive a common reference clock signal. In normal operation, a remote receiver will monitor the facility clock and take a specific action upon recognition of a particular code. Among the many functional characteristics possible for a remote receiver will be for a receiver to start a count of clock pulses. At the conclusion of this count the remote receiver may initiate the transmission of a second code. In this manner various codes could be made to exist in defined time intervals to provide the capability for real time synchronism at various remote locations.

3.2 The Power Conversion Clock output of the FCS will be used for control of a high current power conversion system. The power conversion system will utilize a multiple phase motor generator set as its input. Output control will be accomplished by varying the duty cycle of individual phases. The FCS will facilitate the power conversion system by providing a clock signal whose frequency is directly proportional to the varying frequency counting circuits to provide precise control of the power conversion equipment over the variable frequency range of the motor generator set.

#### 4.0 Basic Features

The Facility Clock System will be comprised of two separate assemblies. The two assemblies are defined as the Clock Generator Module (CGM) and the Clock Encoder Module (CEM). Each assembly shall be housed in a CAMAC module and shall conform to the requirements defined by the CAMAC standard (Reference Document 2.1). The primary input/output of the modules shall be implemented through use of a rear mounted auxiliary connector. Electrical interfaces to the modules front panel will be for monitoring and are referenced as secondary interfaces, and will be primarily used during initial system integration.

##### 4.1 Clock Generator Module (CGM) Model 401-1

The CGM shall be a single width CAMAC module and shall be capable of functioning in a CAMAC crate as a stand alone system. The CGM shall have three separate output signals that are derived from the characteristics of an AC input source signal. The output signals of the CGM are defined as the Power Conversion Clock, the Twelve Phase Clock and the Zero Crossing Clock. Each output of the CGM shall be simultaneously available at the rear auxiliary connector and at a front panel connector. Outputs shall be suitably isolated so that loading factors may be considered independently.

4.1.1 The frequency of the Power Conversion Clock shall be directly proportioned to the frequency of the AC input source in the ratio of 16,668 to 1. Corrections to the output frequency shall be made for each cycle of the source voltage and error shall be accumulated. A possible method of achieving this characteristic is delineated in Figure 10.1. With this method the accumulative counter is not cleared so that no counts are lost over long periods of time. The error counter, however, will be cleared after each input cycle and facilitate more rapid response to changing input source frequency.

4.1.2 The Twelve Phase Clock output shall be a continuous pulse train whose frequency shall be directly proportioned to the frequency of the AC input source in the ratio of 12 to 1. The phasing of this output will be such that every twelfth pulse be coincident with the Zero Crossing Clock.

#### 4.2 Clock Encoder Module (CEM) Model 401-2

The CEM shall be housed in a double width CAMAC module. The module shall have thirty-two "priority level" input ports, an "external clock" input port and one "encoded clock" output port; implemented through the rear auxiliary connector. In addition, one "encoded clock" output port and one "external clock" input port shall be simultaneously available to front panel connectors. All outputs shall be suitably isolated so that loading factors for each may be considered independently. The functional requirement of the CEM is to monitor thirty-two (32) priority level input ports and encode upon the clock a seven (7) bit ASCII character code associated with the highest priority level sensed. In addition, the module shall respond to CAMAC Dataway commands and on a lowest priority level, encode the clock with 8 bits of data transferred from the Dataway. The source of the main data clock shall be selected by switch to be either from an internal 1 MHz oscillator or from an external clock input port.

##### 4.2.1 Priority Level Inputs

Each of the thirty-two (32) priority level input ports shall have a seven (7) bit ASCII character code (as defined by Reference Document 2.3) assigned to it. Upon receipt of an input signal the CEM shall encode upon the clock the associated code. Upon recognition of more than one input signal the module shall first encode the data corresponding to the highest level of priority sensed. Each input port shall have an asynchronous storage cell associated with it. The storage cell shall be "set" upon receipt of input and not "reset" until transmission of the code is complete. The CEM will continue to encode and transmit data until all its input cells are clear.

##### 4.2.2 Dataway Interface

The Dataway Interface shall be a standard CAMAC interface conforming to all requirements of reference 2.1. The module will respond to two CAMAC commands as delineated in section 6.6.1.3.

##### 4.2.3 External Clock Input

The External Clock Input shall be a variable frequency TTL compatible clock. The Clock Encoder Module shall be capable of operating at over the full range of the Power Conversion Clock as defined by Sections 3.2 and 6.5.1.

## 5.0 Mechanical Characteristics

The Clock Generator and the Clock Encoder Module shall be CAMAC modules and conform to the general mechanical requirements outlined in Reference Document 2.1.

5.1 Electrical component mounting for front panels shall be as indicated by applicable Figures 10.2 or 10.3. Circuit board components shall be mounted on a high quality printed circuit board conforming to all the requirements of Reference Document 2.5.

5.2 Mechanical artwork shall be supplied with the modules and shall comply with the requirements of Reference Documents 2.4 and 2.5.

5.3 Auxiliary connectors shall be accessible from the rear of the modules and mounted above the Dataway plug as indicated by Reference Document 2.1, Figures 3 and 4. The CGM shall utilize two thirty-six (36) pin edge type connectors, one (1) in each of two (2) adjacent CAMAC stations. Auxiliary connect shall mate with a Viking connector 3V18 (or equivalent). The card edge connector(s) must be marked with pin 1 on top and pin 18 on the bottom; in addition, the letter 'A' shall be marked on the side of the card adjacent to the next lower numbered CAMAC station.

5.4 Connector pin assignments shall conform to Figure 10.4 and 10.5 as applicable.

## 6.0 Electrical Characteristics

6.1 The modules must conform to the electrical requirements outlined in reference specifications 2.1 and 2.2.

6.2 Input Power shall be derived from the standard + 6 volt and + 24 volt CAMAC supply voltages. Whenever possible, low power circuitry (such as the 74LS series) shall be used to minimize power dissipation.

6.3 The +6 and -6 volt supply voltages must be bypassed on the module with electrolytic capacitors of at least 33 microfarads. The +24 and -24 volt supply voltages must be bypassed with electrolytic capacitors of at least 6.8 microfarads. In addition, at least half the integrated circuits must contain a ceramic bypass capacitor of at least .01 microfarads on their supply voltage lines. The .01 microfarad capacitors should be located as close as possible to the integrated circuits.

6.4 The use of insulated sandwich type busses for carrying the +5 volt and ground lines for TTL logic is strongly encouraged to provide additional noise suppression and to simplify printed circuit layout design.

### 6.5 Clock Generator Module

6.5.1 The CGM shall have one AC input signal. The input shall be a sinusoidal signal with a nominal amplitude of 10 volts RMS. The frequency of the AC input signal shall be variable and be derived either from the public utility line (60 Hz) or from the output of a motor-generator set (50 Hz to 100 Hz). The maximum rate of change shall be 3 Hertz per second over an approximate period of 15 seconds. The input/output transfer ratio shall be 16668 pulses per input cycle, effecting an approximate relationship of 1 MHz to 60 Hz. The module shall make use of transformer coupling for isolation, and utilize filters and/or integrators for noise rejection.

6.5.2 The CGM shall have six (6) output circuits as defined by Section 4.1. The outputs shall be transformer coupled and capable of driving properly selected cable terminated with 50 Ohms. The characteristics of the Power Conversion Clock are depicted by Figure 10.6. The characteristics of the Zero Crossing Clock and the Twelve Phase Clock are depicted by Figure 10.7.

## 6.6 Clock Encoder Module

6.6.1 The Clock Encoder Module shall accommodate thirty-two (32) priority level inputs, one clock input and the standard CAMAC Dataway interface.

6.6.1.1 The clock input shall be a TTL level input, terminated with 50 Ohms. A typical application of this input shall be to interface the CEM with the power conversion clock. An internally mounted switch (not accessible from front panel) will be used to select this input for the facility clock encoding. The CEM shall operate at over the full range of the power conversion clock.

6.6.1.2 The priority level inputs shall be transformer coupled and shall be compatible with a "Standard Timing Pulse" (Reference 2.7).

6.6.1.3 The CEM shall provide for a standard CAMAC Dataway interface and respond to the following commands:

Command #1 - Read Module Number -[F(6)·A(0)]

This command gates the module identification number (decimal 401, binary 00011001001) onto the Dataway read lines R1 through R12 with the LSB on R1.

Command #2 - Write Code - [F(16)·A(0)]

This command writes an 8 bit code from the Dataway write lines W1 through W8. The module will transmit the code received on the Facility Clock on a lowest priority basis. The code received from the Dataway shall be checked for parity and for conflict with dedicated codes (140g through 177g). The module will not respond and will not return X for Dataway "Write Code" commands that violate parity or for those that attempt to write dedicated codes.

The module will return Q as a logical "1" for all addressed commands received.

The module will return X as a logical "1" for command #1 and conditionally as delineated above for command #2.



6.6.2 Clock Encoder Module Outputs (2) shall be TTL compatible and capable of driving a properly selected cable terminated with 50 Ohms. The outputs shall be a serial pulse train encoded in Bi-Phase-Level (or Split Phase, Manchester II + 180) as defined by Reference 2.2, Paragraph 5.5.2.5 and Figure 4. The protocol for the data encoding shall utilize a ten (10) bit frame as shown in Figure 10.8. Each ten bit frame shall consist of a start bit (logic '0') followed by seven data bits (ASCII coded format, LSB first) an "even parity" bit and a stop bit. The module shall transmit a continuous stream of logic "ones" when no data is being transmitted. The on-time mark of the encoded clock group shall be the trailing edge of the Stop bit, and the maximum delay between event occurrence and the on-time mark shall be twelve (12ms) microseconds for the highest priority event when the CEM is not transmitting and twenty-two (22ms) if a code is being transmitted when the event is sensed.

6.7 The Clock Encoder Module shall provide one LED indicator mounted on the front panel. The LED must illuminate for a minimum time of approximately 200 milliseconds. The indicator shall illuminate when N is received.

6.8 All components on this module must have a MTBF rating as specified in reference 2.5.

## 7.0 Environmental Data

7.1 The module must operate, as defined, over an ambient temperature range of 0 to +50°C.

7.2 The module must operate, as defined, over a relative humidity range of 10% to 90%. It is not a requirement that the module operate under conditions of water condensation.

7.3 The module must not be affected by an external magnetic field changing at a maximum rate of 100 gauss per second with a peak magnitude of 50 gauss in any direction.

7.4 The module must operate, as defined, in a radiation environment of 1 rad/second (peak) with a total integrated lifetime dose of 1000 rad.

## 8.0 Safety

All components of this module must be of flame retardant material.

## 9.0 Testing

9.1 The module shall undergo all tests normally performed by the Seller. A description of the test performed on this module and the results obtained shall be furnished by the Seller. Successful performance of the tests does not relieve the Seller of the responsibility of certifying that all requirements specified herein are met.

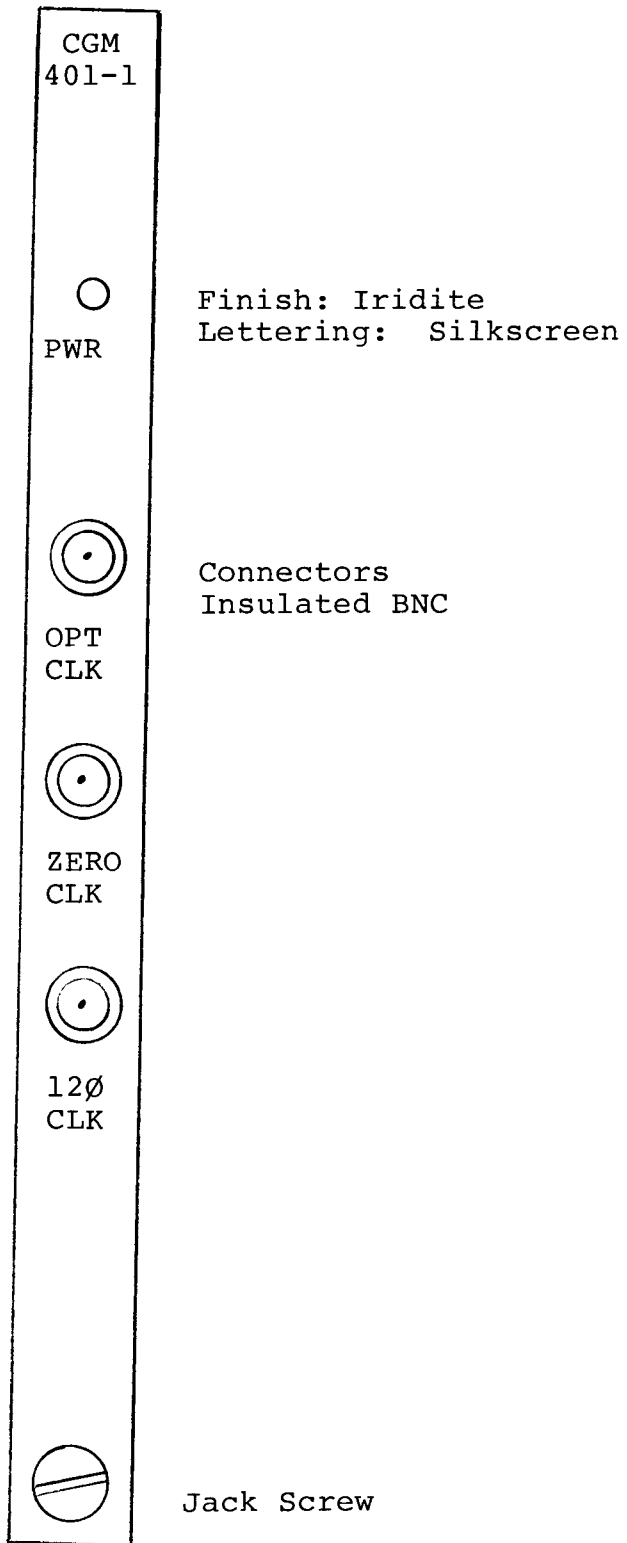


Figure 10.2  
Front Panel Layout  
Clock Generator Module

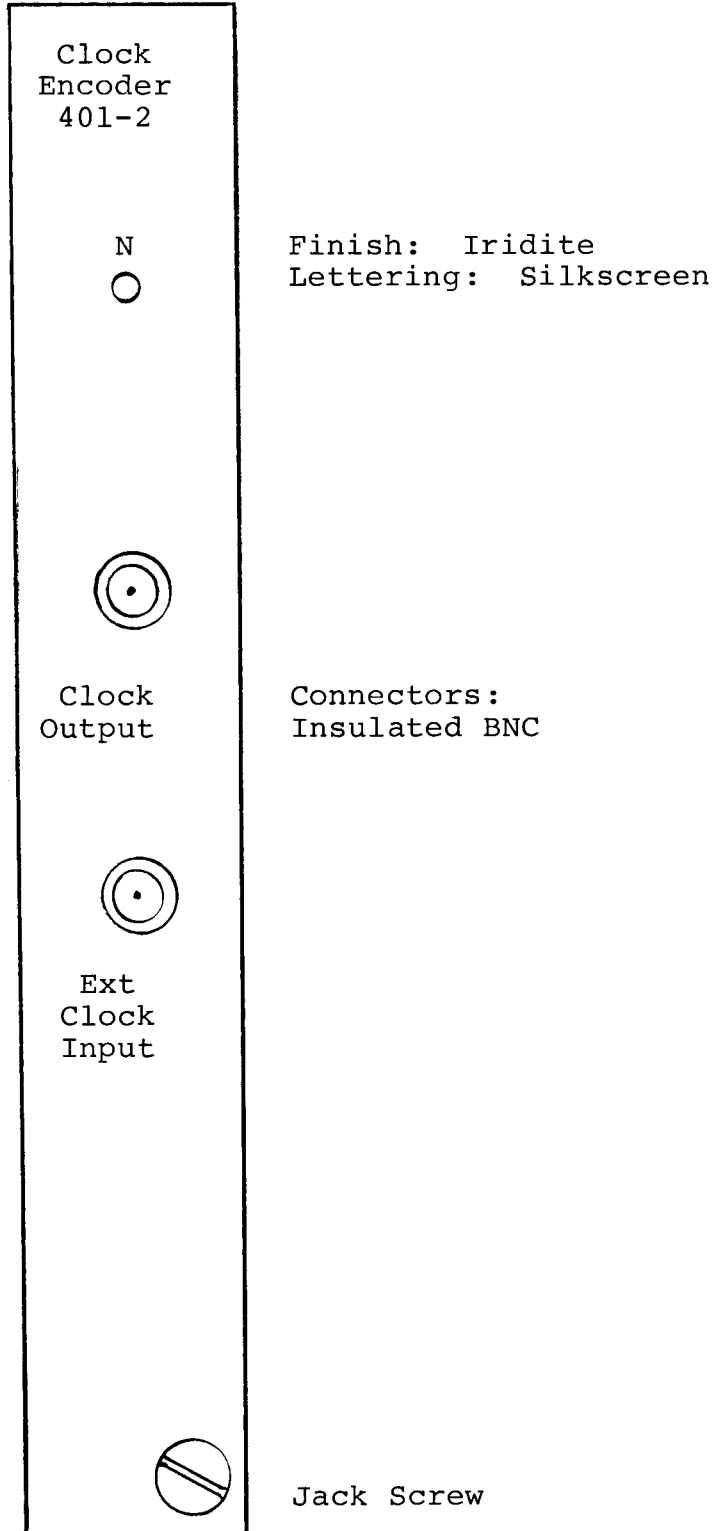


Figure 10.3  
Front Panel Layout  
Clock Encoder Module

AUXILIARY CONNECTOR

(VIEWED FROM FRONT OF CRATE)

PIN DESIGNATION

Input Source Input -----	1B	1A	--- Input Source Return
Clean Earth -----	2B	2A	--- Clean Earth
Output Clock High -----	3B	3A	--- Output CLOck Low
Clean Earth -----	4B	4A	-- Clean Earth
Zero Crossing High ----	5B	5A	-- Zero Crossing Low
Clean Earth -----	6B	6A	-- Clean Earth
12 $\phi$ Clock High -----	7B	7A	-- 12 $\phi$ Clock Low
	8B	8A	
	9B	9A	
	10B	10A	
	11B	11A	
	12B	12A	
	13B	13A	
	14B	14A	
	15B	15A	
	16B	16A	
	17B	17A	
	18B	18A	

FIGURE 10.4

PIN ASSIGNMENT CLOCK GENERATOR MODULE

AUXILIARY CONNECTOR I

(LEFT MOST CONNECTOR VIEWED FROM FRONT OF CRATE)

Priority Input	1	1B	1A	Ret 1
	2	2B	2A	2
	3	3B	3A	3
	4	4B	4A	4
	5	5B	5A	5
	6	6B	6A	6
	7	7B	7A	7
	8	8B	8A	8
	9	9B	9A	9
	10	10B	10A	10
	11	11B	11A	11
	12	12B	12A	12
	13	13B	13A	13
	14	14B	14A	14
	15	15B	15A	15
Priority Input	16	16B	16A	Ret 16
		17B	17A	
		18B	18A	

AUXILIARY CONNECTOR II

(RIGHT MOST CONNECTOR VIEWED FROM FRONT OF CRATE)

Priority Input	17	1B	1A	Ret 17
	18	2B	2A	18
	19	3B	3A	19
	20	4B	4A	20
	21	5B	5A	21
	22	6B	6A	22
	23	7B	7A	23
	24	8B	8A	24
	25	9B	9A	25
	26	10B	10A	26
	27	11B	11A	27
	28	12B	12A	28
	29	13B	13A	29
	30	14B	14A	30
	31	15B	15A	31
Priority Input	32	16B	16A	Ret 32
		17B	17A	
		18B	18A	

FIGURE 10.5  
PIN ASSIGNMENT  
CLOCK ENCODER MODULE

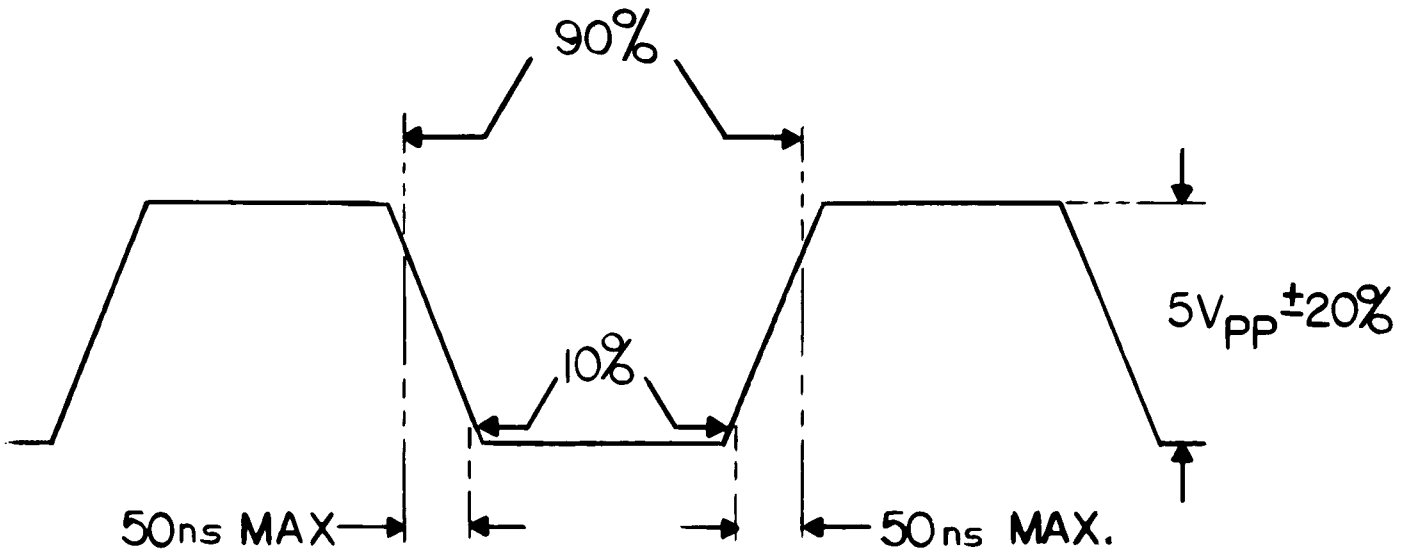


FIG. 10.6  
FACILITY CLOCK CHARACTERISTICS

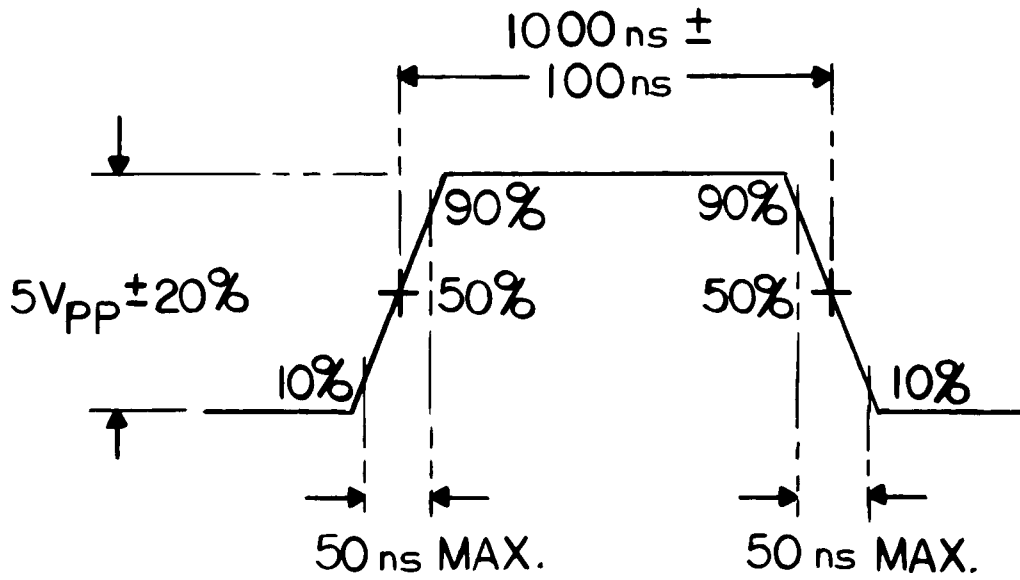


FIG. 10.7  
ZERO CROSSING CLOCK



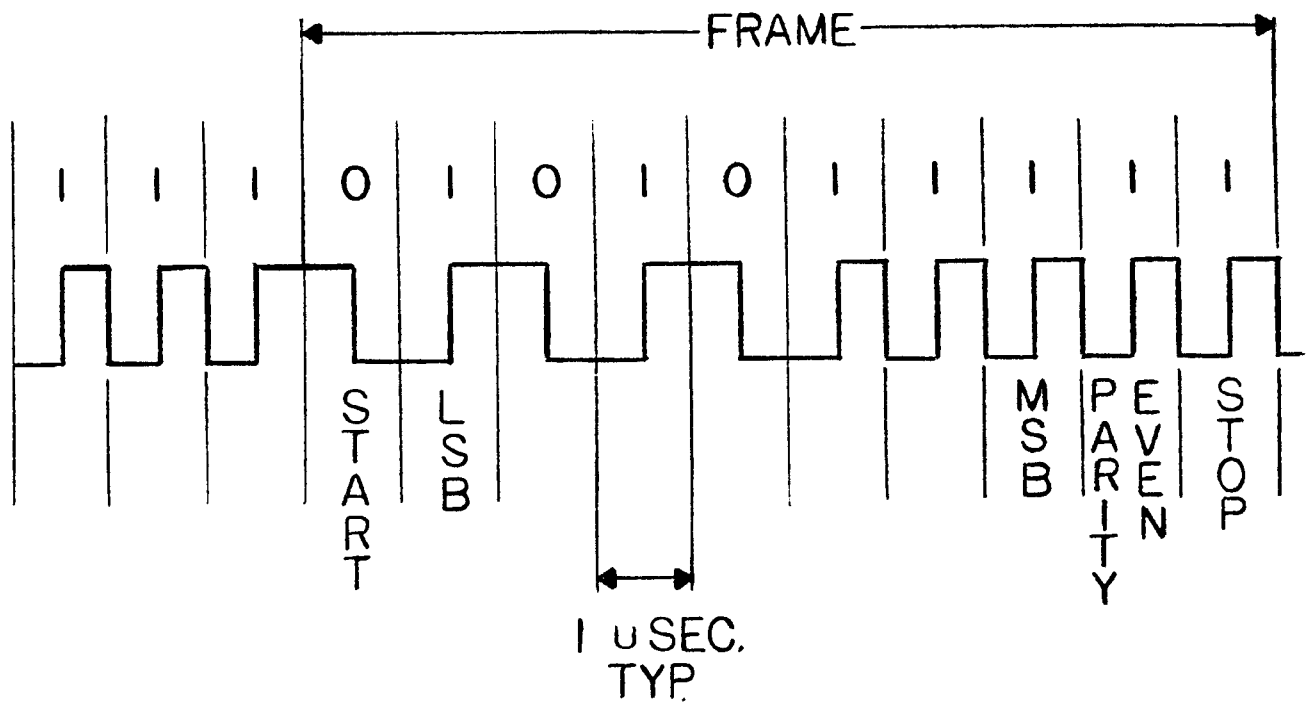


FIG. 10.8 BI-PHASE ENCODED DATA-165

**DIO2**  
**Digital I/O (Timing Module)**

**Hardware Design Description**  
**Documentation**

**CP-DIO2-5023**

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## 0 TABLE OF CONTENTS

<b>1</b>	<b>FUNCTIONAL/LOGICAL DESCRIPTION .....</b>	<b>1-1</b>
1.1	Front and rear digital I/O .....	1-1
1.1.1	Front panel .....	1-2
1.1.2	Rear side .....	1-2
1.2	PXI triggers and timing .....	1-3
1.3	Timing channels .....	1-3
1.3.1	Timing phases .....	1-4
1.3.2	Synchronization Clock .....	1-5
1.4	Connection matrix .....	1-5
1.5	Timing highway .....	1-6
1.6	PCI Controller .....	1-7
<b>2</b>	<b>EXTERNAL INTERFACES .....</b>	<b>2-1</b>
2.1	PCI Addressable Registers .....	2-1
2.1.1	General Control Register (0x000) .....	2-4
2.1.2	General Status Register (0x004) .....	2-5
2.1.3	Clock Control Register (0x008) .....	2-6
2.1.4	Version and Reset Register (0x00C) .....	2-7
2.1.5	I/O Connection Registers, channel 1 to 16 (0x010-04C) .....	2-7
2.1.6	PXI Connection Registers, trigger 0 to 7 (0x050-0x06C) .....	2-8
2.1.7	I/O Register (0x070) .....	2-8
2.1.8	Event Recorder Register (0x074) .....	2-9
2.1.9	Event Recorder Code Register (0x078) .....	2-9
2.1.10	Event Recorder Time Register (0x07C) .....	2-9
2.1.11	Event Code Registers, 1 to 16 (0x080-0x0BC) .....	2-10
2.1.12	Timing Channel Mode Registers, channel 1 to 8 .....	2-11
2.1.13	Phase 1 Cycle Part 1 Registers, channel 1 to 8 .....	2-12
2.1.14	Phase 1 Cycle Part 2 Registers, channel 1 to 8 .....	2-12
2.1.15	Phase 2 Cycle Part 1 Registers, channel 1 to 8 .....	2-12
2.1.16	Phase 2 Cycle Part 2 Registers, channel 1 to 8 .....	2-12
2.1.17	Phase 2 Delay Registers, channel 1 to 8 .....	2-13
2.1.18	Phase 2 Duration Registers, channel 1 to 8 .....	2-13
2.1.19	Phase 1 Counter Status Registers, channel 1 to 8 .....	2-13
2.1.20	Phase 2 Counter Status Registers, channel 1 to 8 .....	2-13
2.1.21	Timing Channel Status Register 1 (0x2C0-2FC) .....	2-14
2.1.22	Timing Channel Status Register 2 (0x300-3FC) .....	2-14
2.2	CompactPCI interface .....	2-15
2.2.1	Mechanical .....	2-15

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2.2.2	Electrical .....	2-15
2.2.3	Functional .....	2-15
2.2.4	Allocation .....	2-15
2.3	PXI interface .....	2-16
2.3.1	Mechanical .....	2-16
2.3.2	Electrical .....	2-16
2.3.3	Functional .....	2-16
2.3.4	Allocation .....	2-16
2.4	Front panel digital in/out .....	2-17
2.4.1	Mechanical .....	2-17
2.4.2	Electrical .....	2-17
2.4.3	Functional .....	2-18
2.4.4	Allocation .....	2-18
2.5	Rear panel digital in/out .....	2-19
2.5.1	Mechanical .....	2-19
2.5.2	Electrical .....	2-19
2.5.3	Functional .....	2-19
2.5.4	Allocation .....	2-20
2.6	Optical In/Out .....	2-21
2.6.1	Mechanical .....	2-21
2.6.2	Optical/Electrical .....	2-21
2.6.3	Logical .....	2-21
2.6.4	Allocation .....	2-22
2.7	LED User Interface .....	2-23
2.7.1	Function .....	2-23
2.7.2	Allocation .....	2-23

### 3 ALLOCATION..... 3-1

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## REVISION HISTORY

Date	Rev.	Prep. by	Comment
2002-05-13	A	REB	<ul style="list-style-type: none"> <li>Initial draft version.</li> </ul>
2002-05-30	A	REB	<ul style="list-style-type: none"> <li>Changed command code of several commands.</li> <li>Added <b>TCGATESYNC</b> to Timing Channel Mode Register.</li> <li>Changed description of the Phase x Cycle Part x Registers.</li> </ul>
2002-05-31	A	REB	<ul style="list-style-type: none"> <li>Added <b>BUSY</b> bit to the General Status Register.</li> <li>Changed <b>TCSCLRON</b> bits to <b>TCSTARTED</b> bits.</li> <li>Removed <b>STATE</b> parameter from the General Status Register.</li> </ul>
2002-06-03	A	REB	<ul style="list-style-type: none"> <li>Changed description of the Phase x Counter Status Registers.</li> <li>Added Event Recorder Register, Event Recorder Code Register and Event Recorder Time Register.</li> <li>Added commands in the General Control Register for Event Recorder control.</li> </ul>
2002-06-07	A	REB	<ul style="list-style-type: none"> <li>Added description of the <b>TCGATE</b> parameter.</li> <li>Address map assignments made.</li> <li>Updated timing channel state diagram.</li> <li>Updated DIO2 block diagram.</li> <li>Added timing channel clock limitation with an external clock.</li> <li>Changed synchronization clock (timing clock) description.</li> </ul>
2002-06-11	A	REB	<ul style="list-style-type: none"> <li>Added <b>CLKOK</b> status bit to the Clock Control Register.</li> <li>Added interrupt generation on Event Recorder FIFO half full.</li> </ul>
2002-06-12	A	REB	<ul style="list-style-type: none"> <li>Removed <b>TCSTARTED</b> bits from Timing Channel Status Register 1 since this information is also in the Timing Channel Status Register 2 under the <b>TCSTATUS</b> bits.</li> </ul>
2002-06-18	A	REB	<ul style="list-style-type: none"> <li>Removed <b>OPTOTXEN</b> bit from the General Control Register.</li> <li>Changed bit positions within General Control Register.</li> </ul>
2002-06-20	A	REB	<ul style="list-style-type: none"> <li>Updated the Note with the Clock Control Register regarding the reset.</li> <li>Corrected <b>CLKSRC</b> parameter description</li> <li>Updated <b>EVENT</b> command description.</li> <li>Updated description of <b>IO50OHM</b> parameter.</li> </ul>
2002-06-27	A	REB	<ul style="list-style-type: none"> <li>Changed timing channel clock limitations with an external clock. The clock frequency must now be four times the desired timing channel frequency.</li> </ul>
2002-06-28	A	REB	<ul style="list-style-type: none"> <li>Added I/O error interrupt in General Status Register and I/O Connection Registers.</li> </ul>
2002-08-06	A	REB	<ul style="list-style-type: none"> <li>Changed the Event Recorder size from 64 to 32.</li> <li>Changed the Event Recorder Register: <b>ERCOUNT</b> is now 6 bits wide and <b>ERINTEN</b> is now located at bit 15.</li> </ul>
2002-10-02	A	REB	<ul style="list-style-type: none"> <li>Added <b>STOP</b> command in General Control Register.</li> <li>Changed <b>ECSTART</b> and <b>ECSTOP</b> bits to <b>ECTIMEEV</b> parameter in Event Code Register.</li> </ul>
2002-11-01	A	REB	<ul style="list-style-type: none"> <li>Added description of the timing channels and the timing highway.</li> </ul>

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Date	Rev.	Prep. by	Comment
2002-11-21	A	REB	<ul style="list-style-type: none"><li>Added description about power up situation of timing highway decoder.</li></ul>
2003-01-03	A	REB	<ul style="list-style-type: none"><li>Added notes to <b>ECEVENT</b> in the Event Code Register.</li><li>Added <b>CLKTHSYNC</b> and <b>CLKTHOUT</b> parameters to the Clock Control Register.</li></ul>
2003-02-17	A	REB	<ul style="list-style-type: none"><li>Added component allocation picture.</li></ul>
2003-05-19	A	REB	<ul style="list-style-type: none"><li>Added some pictures for clarification of the DIO2 features.</li></ul>

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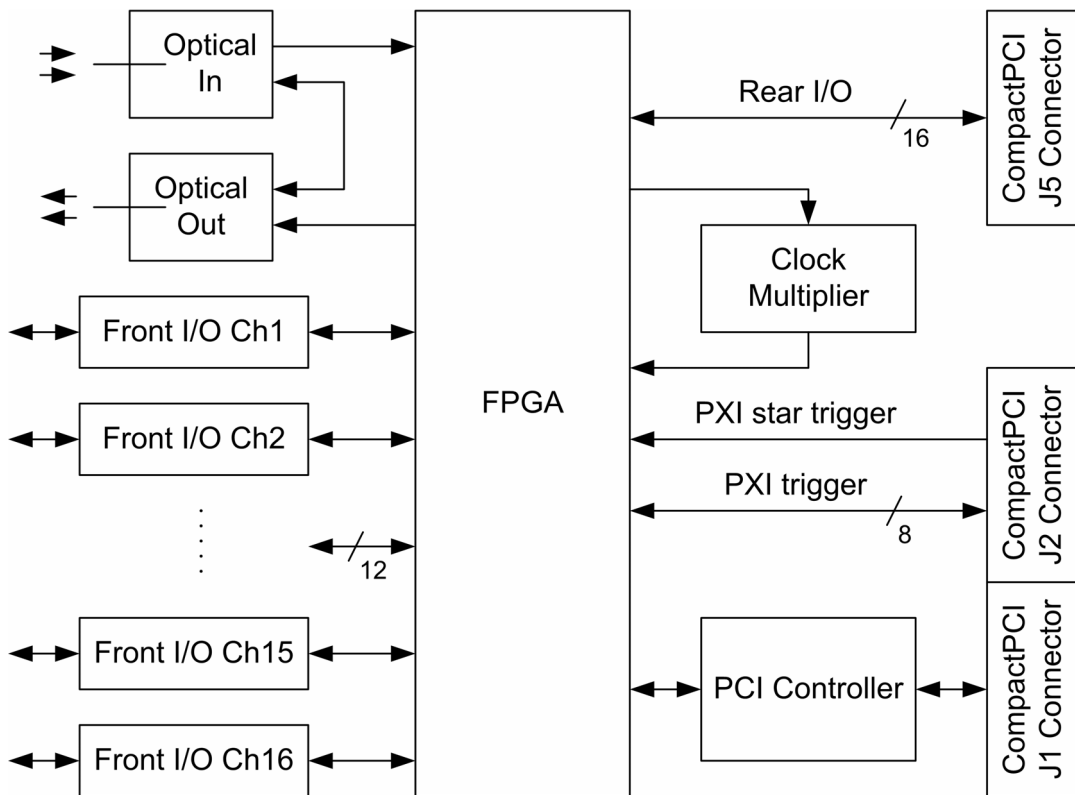


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# 1 FUNCTIONAL/LOGICAL DESCRIPTION

The DIO2 is a general purpose, 16 channel, digital I/O module with 8 flexible assignable timing/trigger channels in a 6U high CompactPCI form factor. The 16 channels can be used via the front panel or the rear side.

The timing channels can be assigned to any of the 16 front or rear side I/Os or to any of the PXI trigger signals. They are synchronized to an external or internal clock.

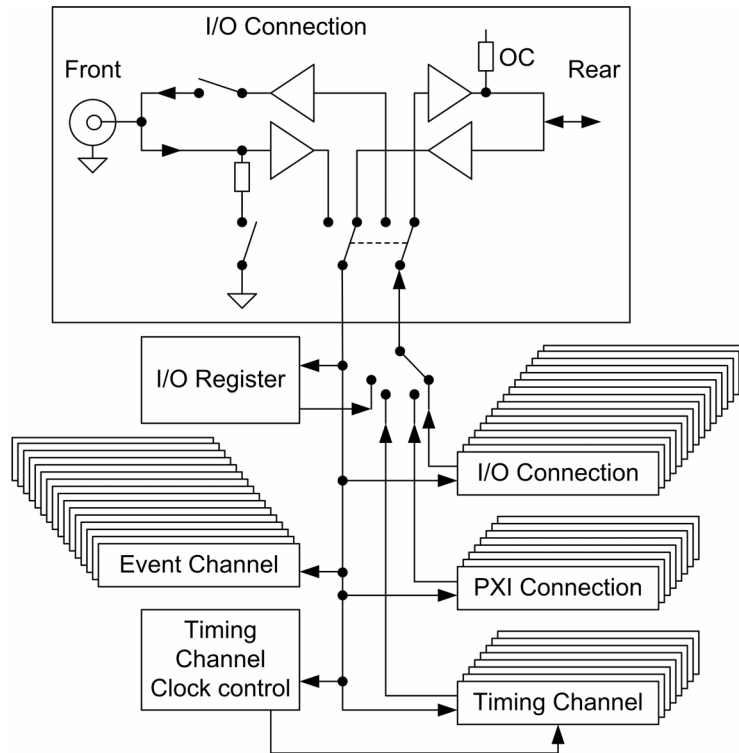


## 1.1 Front and rear digital I/O

The digital I/O channels can work in different modes. The 'normal' transparent mode provides register based direct I/O. In a few different 'buffer' modes, selected signals can be buffered to other outputs to provide, for example, a star trigger or timing geometry. And there is the 'timing' mode in which, a selected (one of eight) timing channels can be assigned to one or more outputs.

The DIO2 is a 16 channel digital I/O module and therefore each channel can have its source and destination on the front or the rear side of the module. When the front is selected the rear side is ignored and vice versa.

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### 1.1.1 Front panel

The front digital output is capable of driving a 50Ω load. When needed a 50Ω input termination can be selected. This input termination can be switched on or off by register access.

Since the I/O buffer circuit can be used as an input and an output, an extra protection has been build in. When the clock buffer is set to be an output, the input is read back and compared to the driven level. When these are not equal the output is disabled and an error is indicated through a front LED, a status bit and/or an interrupt.

### 1.1.2 Rear side

There are digital inputs and output on the rear side of the module. The rear digital output is an open-collector output with a 10kΩ pull-up. In this way it can be used on a transition module without problems. It can even be bussed up to 8 loads (when all have a 10kΩ pull-up). These outputs are not capable of driving a cable of any sort. A transition module mounted on the rear side of CompactPCI, should provide appropriate cable drivers when needed.

The inputs are 5V tolerant and are always enabled.

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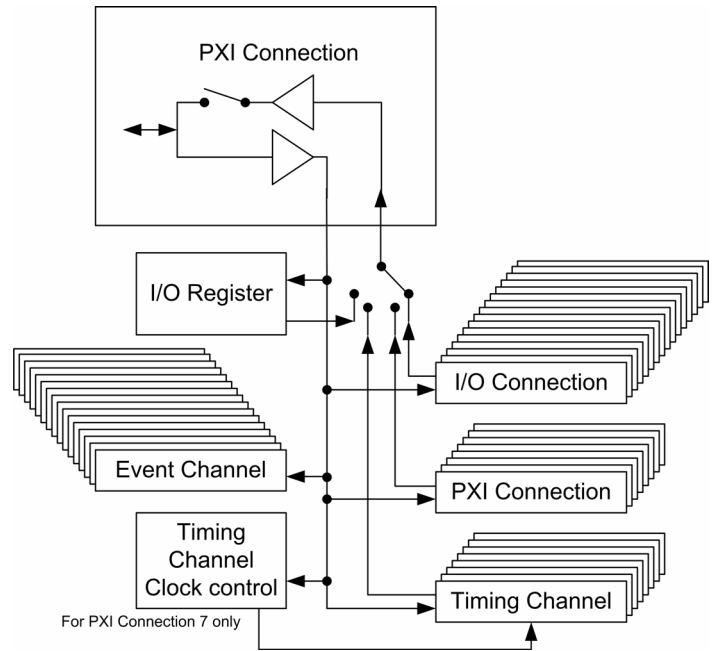
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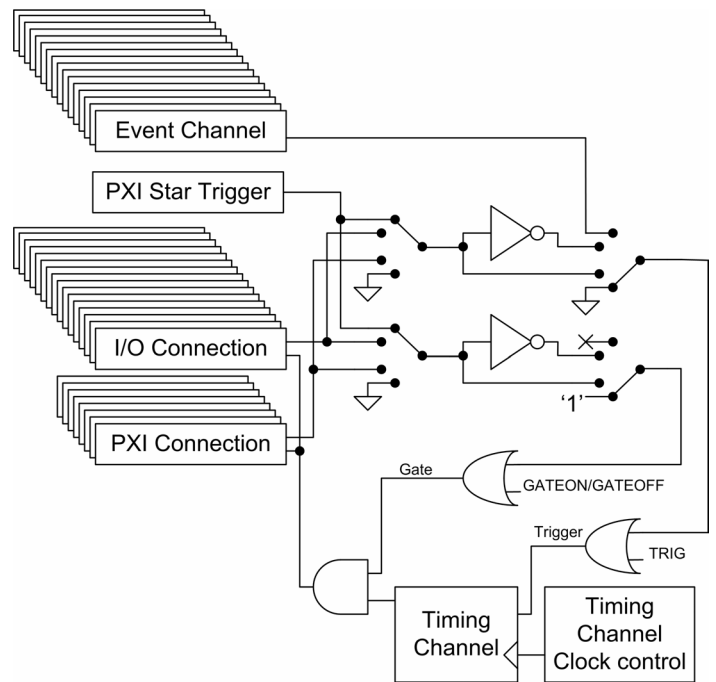
## 1.2 PXI triggers and timing

The PXI interface consists of 8 PXI trigger signals and one PXI star trigger input. PXI trigger signals can be defined as input or output and can work in different modes also. The 'normal' transparent mode provides register based direct I/O. Two 'buffer' modes are available where selected front or rear signals can be buffered to the PXI triggers. And there is the 'timing' mode in which, a selected (one of eight) timing channel can be assigned to one or more PXI trigger outputs. One PXI trigger signal (**PXI\_TRIG7**) is especially designed to transport a clock to other modules.



## 1.3 Timing channels

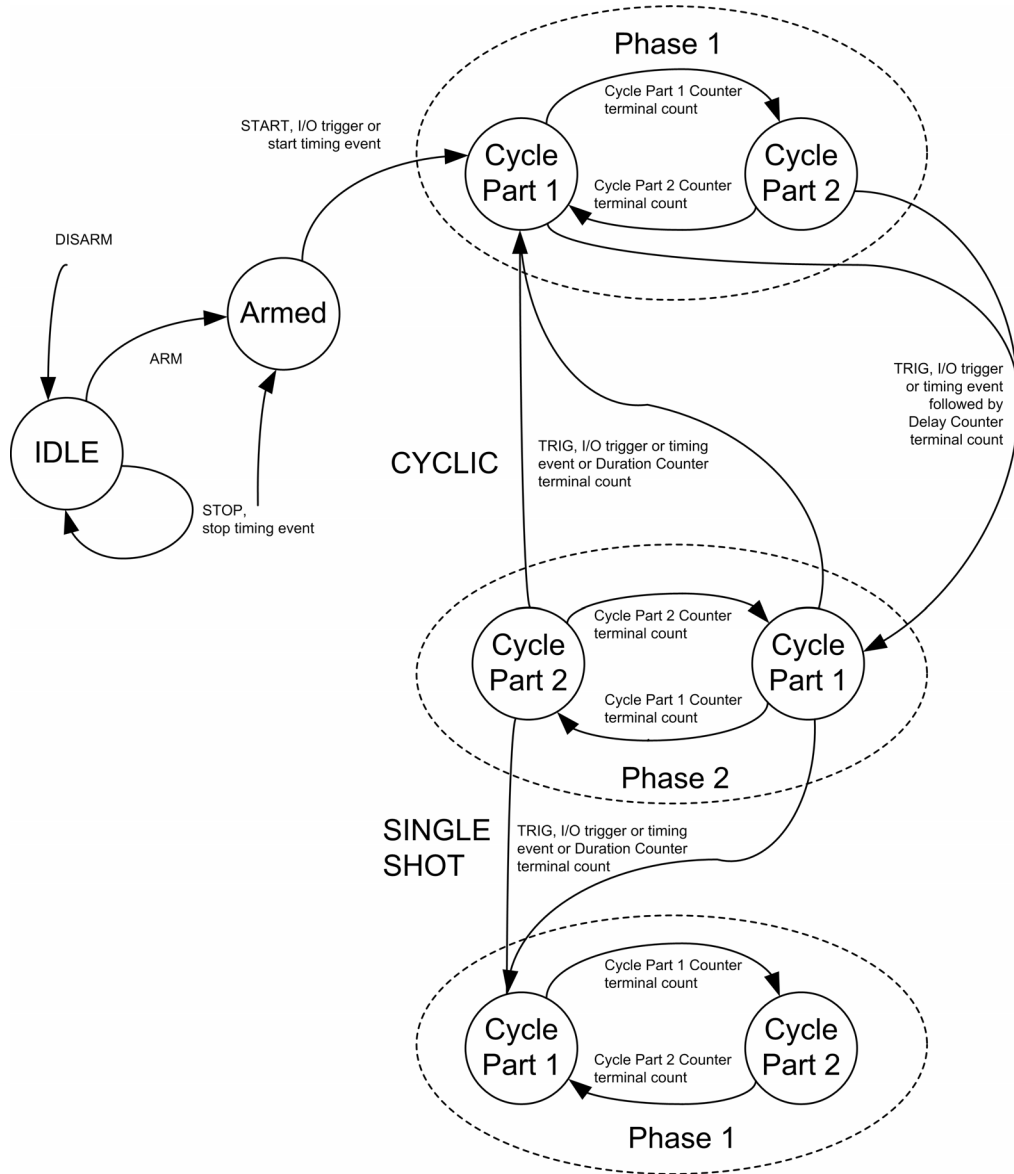
The 8 different timing channels can be assigned to one or more digital I/Os (front and/or rear) or one or more PXI trigger signals. The 8 timing channels have a multiple phase configuration. The change from one phase to the next can be controlled using different triggers, which can be selected per timing channel. Triggers like: software trigger, front/rear I/O and PXI trigger, and the PXI star trigger are available. A timing event, received via the optical input can also be used as a trigger for the timing channel. The timing channels can also be gated. This gate can be a software gate, a front/rear I/O and PXI trigger signal, or the PXI star trigger signal.



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### 1.3.1 Timing phases

The timing channels have two phases. During each phase a periodic signal can be generated. This periodic signal consist of two cycle parts of which the duration and the output level can be defined. So it is possible to create clock signals, DC levels and pulses.



When the timing channel has been armed it can be started using a **START** command, a trigger or a timing event (general or start). The timing channel always starts in **Phase 1**. The output signals alternates between the levels of cycle part 1 and cycle part 2 until the timing channel changes over to **Phase 2**.

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This change over will take place after a trigger and a specified delay (which can be 0). During Phase 2 the output signals alternates between the levels of cycle part 1 and cycle part 2 of phase 2. A Change over from Phase 2 back to Phase 1 can occur after another trigger or after a specified duration. When the timing channel is in cyclic mode it can be retriggered to change over to Phase 2 again. In non-cyclic mode (single shot) the timing channel will remain in Phase 1 and can not be retriggered.

### 1.3.2 Synchronization Clock

The timing channels will operate synchronously to a selected clock. This can be an internal 40MHz clock, an externally provided clock (through PXI, front or rear I/O) or though the optical Timing highway. The Timing high way clock is (normally) 1MHz and is multiplied onboard to the required 40MHz. The timing channels output are timed on a 10MHz clock, which is the mentioned 40MHz divided by four. When an external clock is used (PXI, front or rear I/O) the clock must be four times the needed clock. The external clock frequency may not be higher than 40MHz or 20MHz depending on the selected clock.

## 1.4 Connection matrix

As stated before the front, rear and PXI I/O can work in different modes by which connection between different functional parts of the DIO2 can be made.

	To	Register	Front/Rear Out ch. 1 to 16	PXI trigger 0 to 7	Trigger Timing ch. 1 to 8	Gate Timing ch. 1 to 8
<b>Register</b>	Via I/O	✓	✓	✓		
<b>Front/Rear In ch. 1 to 16</b>	✓	✓	✓	✓	✓	✓
<b>PXI trigger 0 to 7</b>	✓	✓			✓	✓
<b>PXI star trigger</b>					✓	✓
<b>Trigger Timing ch. 1 to 8</b>	✓	✓	✓	✓	Via I/O	Via I/O
<b>TRIG command</b>					✓	
<b>GATE command</b>						✓

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**Note:** The timing channels can be gated and/or triggered by other timing channels when the timing channel output is directed via a front, rear or PXI output and input, to another timing channel.

## 1.5 Timing highway

The timing highway is an optically received, bi-phase encoded (Manchester encoded), signal. Which, because it is bi-phase encoded, results in a clock of 1MHz when no data is received. A rising edge within the middle of a 1µs period represents a logical '0' and a falling edge a logical '1'. During idle state a logical '1' is bi-phase encoded.

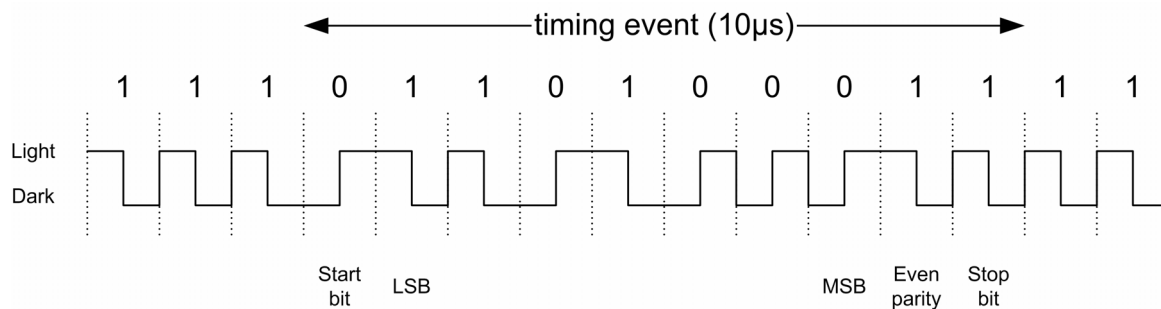
When data is received this will be a timing events which can be used as a trigger of the timing channels.

The received event can also be recorded in a 32 events deep FIFO including a time stamp.

The DIO2 is also capable of encoding and transmitting timing highway events. A software command or a selected trigger can cause the transmission of a timing event.

The encoded timing highway signal starts with a start bit (logical '0'), followed by 7 data bits (LSB first), a even parity bit and a stop bit (logical '1'). Because 1 bit lasts 1µs the transmission of a timing event takes 10µs.

An example of the timing highway signal can be seen below.



The 1MHz clock which is encoded in the signal at all times is decoded out of the timing highway signal and can be used (multiplied by 10) to clock the timing channels with.

During power up of the DIO2 it is possible that part of the design which extracts the 1MHz clock out of the timing highway signal locks on the falling edges in the middle of a '0' instead of the falling edges at the start of a '1'.

The DIO2 is capable of detecting this situation when valid data is received. To force this, a timing event with an event code 0x00 can be transmitted along the timing highway.



## 1.6 PCI Controller

The interface with the PCI bus is realized with a PLX 9054 32-bit, 33 MHz PCI bus interface chip. This chip is the interface between the PCI bus and the FPGA. The FPGA is connected to the PCI interface through a local bus. During an access on PCI, the PCI interface chip decides if the local bus should be accessed or not. In case a register is accessed that resides inside the FPGA an access is performed on the local bus. During a write cycle the data is copied from the local bus into the FPGA and during a read cycle the data is copied from the FPGA to the local bus.



## 2 EXTERNAL INTERFACES

In the tables, within this subsection, the R/W column can contain the following information.

R/W column contents	Description
R/W	Readable and Writable
R	Read only
W	Write only
CR	Clearing Read (clears bit after read)
CW	Clearing Write (bit is cleared right after a write to it)

### 2.1 PCI Addressable Registers

Address	Description	R/W
0x000	General Control Register	R/W/CW
0x004	General Status Register	R
0x008	Clock Control Register	R/W
0x00C	Version and Reset Register	R/CW
0x010	I/O Connection Register	Channel 1 R/W
0x014	I/O Connection Register	Channel 2 R/W
0x018	I/O Connection Register	Channel 3 R/W
0x01C	I/O Connection Register	Channel 4 R/W
0x020	I/O Connection Register	Channel 5 R/W
0x024	I/O Connection Register	Channel 6 R/W
0x028	I/O Connection Register	Channel 7 R/W
0x02C	I/O Connection Register	Channel 8 R/W
0x030	I/O Connection Register	Channel 9 R/W
0x034	I/O Connection Register	Channel 10 R/W
0x038	I/O Connection Register	Channel 11 R/W
0x03C	I/O Connection Register	Channel 12 R/W
0x040	I/O Connection Register	Channel 13 R/W
0x044	I/O Connection Register	Channel 14 R/W
0x048	I/O Connection Register	Channel 15 R/W
0x04C	I/O Connection Register	Channel 16 R/W
0x050	PXI Connection Register	Trigger 0 R/W
0x054	PXI Connection Register	Trigger 1 R/W
0x058	PXI Connection Register	Trigger 2 R/W
0x05C	PXI Connection Register	Trigger 3 R/W
0x060	PXI Connection Register	Trigger 4 R/W
0x064	PXI Connection Register	Trigger 5 R/W
0x068	PXI Connection Register	Trigger 6 R/W
0x06C	PXI Connection Register	Trigger 7 R/W
0x070	I/O Register	R/W
0x074	Event Recorder Register	R/W
0x078	Event Recorder Code Register	R
0x07C	Event Recorder Time Register	R

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Address	Description	R/W
0x080	Event Code Register 1	R/W
0x084	Event Code Register 2	R/W
0x088	Event Code Register 3	R/W
0x08C	Event Code Register 4	R/W
0x090	Event Code Register 5	R/W
0x094	Event Code Register 6	R/W
0x098	Event Code Register 7	R/W
0x09C	Event Code Register 8	R/W
0x0A0	Event Code Register 9	R/W
0x0A4	Event Code Register 10	R/W
0x0A8	Event Code Register 11	R/W
0x0AC	Event Code Register 12	R/W
0x0B0	Event Code Register 13	R/W
0x0B4	Event Code Register 14	R/W
0x0B8	Event Code Register 15	R/W
0x0BC	Event Code Register 16	R/W
0x0C0-0x0DC	Timing Channel Mode Register	R/W
0x0E0	Phase 1 Cycle Part 1 Register	R/W
0x0E4	Phase 1 Cycle Part 2 Register	R/W
0x0E8	Phase 2 Cycle Part 1 Register	R/W
0x0EC	Phase 2 Cycle Part 2 Register	R/W
0x0F0	Phase 2 Delay Register	R/W
0x0F4	Phase 2 Duration Register	R/W
0x0F8	Phase 1 Counter Status	R
0x0FC	Phase 2 Counter Status	R
0x100-0x11C	Timing Channel Mode Register	R/W
0x120	Phase 1 Cycle Part 1 Register	R/W
0x124	Phase 1 Cycle Part 2 Register	R/W
0x128	Phase 2 Cycle Part 1 Register	R/W
0x12C	Phase 2 Cycle Part 2 Register	R/W
0x130	Phase 2 Delay Register	R/W
0x134	Phase 2 Duration Register	R/W
0x138	Phase 1 Counter Status	R
0x13C	Phase 2 Counter Status	R
0x140-0x15C	Timing Channel Mode Register	R/W
0x160	Phase 1 Cycle Part 1 Register	R/W
0x164	Phase 1 Cycle Part 2 Register	R/W
0x168	Phase 2 Cycle Part 1 Register	R/W
0x16C	Phase 2 Cycle Part 2 Register	R/W
0x170	Phase 2 Delay Register	R/W
0x174	Phase 2 Duration Register	R/W
0x178	Phase 1 Counter Status	R
0x17C	Phase 2 Counter Status	R
0x180-0x19C	Timing Channel Mode Register	R/W
0x1A0	Phase 1 Cycle Part 1 Register	R/W
0x1A4	Phase 1 Cycle Part 2 Register	R/W
0x1A8	Phase 2 Cycle Part 1 Register	R/W
0x1AC	Phase 2 Cycle Part 2 Register	R/W
0x1B0	Phase 2 Delay Register	R/W
0x1B4	Phase 2 Duration Register	R/W
0x1B8	Phase 1 Counter Status	R
0x1BC	Phase 2 Counter Status	R

Address	Description	R/W
0x1C0-0x1DC	Timing Channel Mode Register	R/W
0x1E0	Phase 1 Cycle Part 1 Register	R/W
0x1E4	Phase 1 Cycle Part 2 Register	R/W
0x1E8	Phase 2 Cycle Part 1 Register	R/W
0x1EC	Phase 2 Cycle Part 2 Register	R/W
0x1F0	Phase 2 Delay Register	R/W
0x1F4	Phase 2 Duration Register	R/W
0x1F8	Phase 1 Counter Status	R
0x1FC	Phase 2 Counter Status	R
0x200-0x21C	Timing Channel Mode Register	R/W
0x220	Phase 1 Cycle Part 1 Register	R/W
0x224	Phase 1 Cycle Part 2 Register	R/W
0x228	Phase 2 Cycle Part 1 Register	R/W
0x22C	Phase 2 Cycle Part 2 Register	R/W
0x230	Phase 2 Delay Register	R/W
0x234	Phase 2 Duration Register	R/W
0x238	Phase 1 Counter Status	R
0x23C	Phase 2 Counter Status	R
0x240-0x25C	Timing Channel Mode Register	R/W
0x260	Phase 1 Cycle Part 1 Register	R/W
0x264	Phase 1 Cycle Part 2 Register	R/W
0x268	Phase 2 Cycle Part 1 Register	R/W
0x26C	Phase 2 Cycle Part 2 Register	R/W
0x270	Phase 2 Delay Register	R/W
0x274	Phase 2 Duration Register	R/W
0x278	Phase 1 Counter Status	R
0x27C	Phase 2 Counter Status	R
0x280-0x29C	Timing Channel Mode Register	R/W
0x2A0	Phase 1 Cycle Part 1 Register	R/W
0x2A4	Phase 1 Cycle Part 2 Register	R/W
0x2A8	Phase 2 Cycle Part 1 Register	R/W
0x2AC	Phase 2 Cycle Part 2 Register	R/W
0x2B0	Phase 2 Delay Register	R/W
0x2B4	Phase 2 Duration Register	R/W
0x2B8	Phase 1 Counter Status	R
0x2BC	Phase 2 Counter Status	R
0x2C0-0x2FC	Timing Channel Status Register 1	R
0x300-0x3FC	Timing Channel Status Register 2	R

Higher addresses contain the same registers because only the least significant 10 address lines are used.

Because the registers are always addressed as 32 bits registers the least significant 2 address lines are not monitored.



## 2.1.1 General Control Register (0x000)

Bit	Description	R/W	Reset
3:0	<b>COMMAND</b> ; Command given to the DIO2 to specify its operation. See also the <b>BUSY</b> bit in the General Status Register.	R/CW	0
11:4	<b>OPERANT</b> ; Extra parameter used with <b>COMMAND</b> .	R/CW	0
12	<b>IOERRCLR</b> ; Clears the I/O error status. This means clearing the I/O error status bits, enabling front outputs and changing the LED status from red to yellow/orange.	R/CW	0
13	<b>INTCLR</b> ; Remove the generated PCI interrupt.	R/CW	0
31:14	Reserved	R	0

The following values are valid commands, which can be assigned to the **COMMAND** parameter.

COMMAND	Description	Valid in TCSTATUS
0000 (0x0)	Has no function	All
1110 (0xE)	<b>DISARM</b> ; Disarm one or more timing channels. The selected timing channels are placed in the IDLE state immediately. The channel selection (1 to 8) must be entered in the <b>OPERANT</b> parameter.	ARMED, PHASE1, PHASE2
0001 (0x1)	<b>ARM</b> ; Arm one or more timing channels so they are ready to receive triggers. The scalers/counters are <u>not</u> started in any situation (see <b>START</b> command). The channel selection (1 to 8) must be entered in the <b>OPERANT</b> parameter.	IDLE
0010 (0x2)	<b>START</b> ; Start the selected timing channels. This can be used when, for a channel no start event has been defined. The timing channel goes to the PHASE1 state. The channel selection (1 to 8) must be entered in the <b>OPERANT</b> parameter.	ARMED
1101 (0xD)	<b>STOP</b> ; Stop the selected timing channels. This can be used when, for a channel no stop event has been defined. The timing channel goes back to the ARMED state. The channel selection (1 to 8) must be entered in the <b>OPERANT</b> parameter.	PHASE1, PHASE2
0011 (0x3)	<b>TRIG</b> ; Generate a software trigger for one or more timing channels. The channel selection (1 to 8) must be entered in the <b>OPERANT</b> parameter.	ARMED, PHASE1, PHASE2
1010 (0xA)	<b>GATEOFF</b> ; Make the Timing channel gate signal inactive for one or more timing channels. The channel selection (1 to 8) must be entered in the <b>OPERANT</b> parameter.	IDLE, ARMED, PHASE1, PHASE2
1011 (0xB)	<b>GATEON</b> ; Make the Timing channel gate signal active for one or more timing channels. The channel selection (1 to 8) must be entered in the <b>OPERANT</b> parameter.	IDLE, ARMED, PHASE1, PHASE2
1111 (0xF)	<b>EVENT</b> ; generate a timing event. The timing event number must be entered in the <b>OPERANT</b> parameter (the most significant bit of <b>OPERANT</b> is ignored). At least one Event Code Register must be configured as output to enable the optical transmission. When all Event Code Register are configured as input the use of event only affects this module.	IDLE, ARMED, PHASE1, PHASE2
0100 (0x4)	<b>STOPREC</b> ; Stop recording timing events.	All
0101 (0x5)	<b>ARMREC</b> ; Arm the timing event recorder so it can start recording timing events after receiving a recorder start timing event.	All
0111 (0x7)	<b>FLUSHREC</b> ; Remove all recorded timing events.	All

For the commands TRIG, START, STOP, GATEON and GATEOFF the **OPERANT** parameter must be used for the channel selection. The least significant bit of **OPERANT** indicates timing channel 1 and the most significant bit indicates timing channel 8. So every individual timing channel can be accessed one at a time, all at once or just a selection.

## 2.1.2 General Status Register (0x004)

Bit	Description	R/W	Reset
0	<b>BUSY</b> ; A command entered in the General Control Register is being processed. Further commands are ignored when <b>BUSY</b> is set. Because the timing channels are working at a different clock rate than the CompactPCI (local bus) side the entered command has to be synchronized which takes some time during which new commands can not be entered. <b>BUSY</b> is active for a maximum time of 200ns.	R	0
1	<b>TCINTEVENT</b> ; PCI interrupt event has been generated after receiving a trigger, which affected one of the timing channel. Which timing channel has caused the interrupt can be found in the Timing Channel Status Register 1.	R	0
2	<b>RECINTEVENT</b> ; PCI interrupt event has been generated because the event recorder FIFO is half full.	R	0
3	<b>IOERRINTEVENT</b> ; PCI interrupt event has been generated because a front I/O error has occurred.	R	0
7:4	Reserved	R	0
8	<b>OPTOPARERR</b> ; Parity error on the received timing highway event code.	R	0
15:9	Reserved	R	0
31:16	<b>IOERR</b> ; A short circuit has been detected on one or more of the two front panel I/O connectors. The least significant bit of IOERR indicates an error on I/O channel 1, the most significant bit on channel 16.	R	0

## 2.1.3 Clock Control Register (0x008)

Bit	Description	R/W	Reset
1:0	<b>CLKSRC</b> ; The selection of the timing channel clock source. 00 = Internal Clock 01 = Front/Rear I/O external clock 10 = PXI_TRIG7 11 = Timing Highway	R/W	00
5:2	<b>CLKCH</b> ; Selection of the channel when <b>CLKSRC</b> is set to the values 10 (= external clock). 0x0 is channel 1 (front or rear) and 0xF is channel 16 (front or rear).	R/W	0
6	<b>CLKEDGE</b> ; Selection of the active clock edge of the clock source. 0 = Rising edge. 1 = Falling edge.	R/W	0
7	<b>CLKOK</b> ; The selected clock is present. When this bit is cleared the clock is not present or active, or the clock frequency is below 150kHz.	R	0
8	<b>CLKTHSYNC</b> ; Synchronize the (re)generated Timing highway clock/data output signal to the received Timing highway input signal. The delay between the received clock and regenerated clock will be about 100ns. The jitter will be 25ns maximum.	R/W	0
9	<b>CLKTHOUT</b> ; Enable the Timing highway output even when only Event decoders (see Event Code Registers) are used. When encoders are used, this parameter has no effect.	R/W	0
31:8	Reserved	R	0

CLKSRC	IOCH	Description
00	XXXX	Internal Clock
01	0000 – 1111	Front/Rear panel digital I/O channel 1 to 16
10	XXXX	PXI Trigger input signal PXI_TRIG7
11	0000 – 0111	Timing channel 1 to 8
11	1000 – 1111	Timing channel 1 to 8

**Note:** During and after the change of the timing channel clock source the parts of the design, which use this clock, will be resetted. This will also cause the **CLKOK** bit to be cleared until this reset is inactive again and a clock edge had been detected. When the Timing Highway is used as clock source the derived clock will be synchronized to the Timing Highway clock during this reset period. When the Timing Highway clock is not present during this clock source selection there could be a clock skew of 75ns (max) between DIO2s.

**Note:** When PXI\_TRIG7 or the Front/Rear I/O external clock is used these clocks must be four times the desired frequency. So for example with a timing channel clock of 10MHz, PXI\_TRIG7 must run at 40MHz. The maximum allowable frequency of PXI\_TRIG7 is 40MHz. The Rear I/O clock maximum is 20MHz, and the maximum allowable frequency of the Front I/O clock is 10MHz. This would result in a timing channel clock of 5MHz max.

## 2.1.4 Version and Reset Register (0x00C)

Bit	Description	R/W	Reset
7:0	<b>REVISION</b> ; ASCII character '0'	R	0x30
15:8	<b>VERSION</b> ; ASCII character 'A'	R	0x41
23:16	<b>2</b> ; ASCII character '2'	R	0x32
31:24	<b>DIO</b> ; ASCII character 'D'	R	0x44

Bit	Description	R/W	Reset
0	<b>RESET</b> ; When this bit is set the DIO2 will be resetted locally. FIFOs and memories are flushed and all parameters are cleared.	CW	n.a
31:1	Reserved	W	n.a

## 2.1.5 I/O Connection Registers, channel 1 to 16 (0x010-04C)

Bit	Description	R/W	Reset
0	<b>IODIR</b> ; Selection of the direction between input and output. 0 = Input 1 = Output When the <b>IODIR</b> is set to 'Output' all 'Input' features will remain functional and available.	R/W	0
1	<b>IOSIDE</b> ; Which I/O side is used. 0 = Front: Input comes from front and output goes to front digital I/O. 1 = Rear: Input comes from rear and output goes to rear digital I/O.	R/W	0
3:2	<b>IOSRC</b> ; Source of the output signal. 00 = Register: Writing to the I/O register will affect the output. 01 = Buffer: Copy the signal of a front or rear input. 10 = PXI trigger input. The PXI trigger input signal is buffered to the Front or Rear output, dependant on <b>IOSIDE</b> . 11 = Timing channel.	R/W	0
7:4	<b>IOCH</b> ; Selection of the channel when <b>IOSRC</b> is not set to 00 (= Register).	R/W	0
8	<b>IO50OHM</b> ; Select the 50Ω input termination for the front input. This bit is only functional when the front I/O is set to Input. However it can be used with all settings of <b>IODIR</b> and <b>IOSIDE</b> , but is ignored when the front side output is used since input termination on an output is illegal.	R/W	0
9	<b>IOERRINTEN</b> ; Enable PCI interrupt generation after detecting a front I/O error on this I/O channel.	R/W	0
31:10	Reserved	R	0

IOSRC	IOCH	Description
00	XXXX	Register to output
01	0000 – 1111	Front/Rear panel digital I/O channel 1 to 16
10	0000 – 0111	PXI Trigger input signals PXI_TRIG0 to PXI_TRIG7
10	1000 – 1111	PXI Trigger input signals PXI_TRIG0 to PXI_TRIG7
11	0000 – 0111	Timing channel 1 to 8
11	1000 – 1111	Timing channel 1 to 8

## 2.1.6 PXI Connection Registers, trigger 0 to 7 (0x050-0x06C)

Bit	Description	R/W	Reset
0	<b>PXIDIR</b> ; Selection of the direction between input and output. 0 = Input 1 = Output When the direction is set to 'Output' all 'Input' features will remain functional and available.	R/W	0
2:1	<b>PXISRC</b> ; Source of the output signal. 00 = Register: Writing to the I/O register will affect the output. 01 = Buffer: Copy the signal of a front or rear input. 10 = Reserved 11 = Timing channel.	R/W	0
6:3	<b>PXICH</b> ; Selection of the channel when <b>PXISRC</b> is not set to 00 (= Register).	R/W	0
31:7	Reserved	R	0

PXISRC	PXICH	Description
00	XXXX	Register to output
01	0000 – 1111	Front/Rear panel digital I/O channel 1 to 16
10	XXXX	Reserved
11	0000 – 0111	Timing channel 1 to 8
11	1000 – 1111	Timing channel 1 to 8

## 2.1.7 I/O Register (0x070)

Bit	Description	R/W	Reset
15:0	<b>IO</b> ; When writing to <b>IO</b> the Front or Rear outputs are changed when they are configured as output and their source is the I/O register. When reading, the input value from the Front or Rear is read, depending on <b>IOSIDE</b> .	R/W	0
23:16	<b>PXIIO</b> ; When writing to <b>PXIIO</b> the PXI outputs are changed when they are configured as output and their source is the I/O register. When reading, the input value from the PXI trigger inputs is read.	R/W	0
31:24	Reserved	R	0



## 2.1.8 Event Recorder Register (0x074)

Bit	Description	R/W	Reset
6:0	<b>EREVENT</b> ; Timing event code, which starts the recording of all further received timing events.	R/W	0
8:7	<b>ERSTATUS</b> ; The timing event recorder current status. 00 = Idle (stopped). 01 = Armed. 10 = Recording. 11 = Paused because FIFO is full. See General Control Register for Event Recorder specific commands.	R	0
14:9	<b>ERCOUNT</b> ; Counts number of recorded events. The maximum is 32. <b>ERCOUNT</b> is decreased after reading the Event Recorder Code Register.	R	0
15	<b>ERINTEN</b> ; Enable PCI interrupt generation when the event recorder FIFO is half full.	R/W	0
31:16	Reserved	R	0

## 2.1.9 Event Recorder Code Register (0x078)

Bit	Description	R/W	Reset
6:0	<b>ERCODE</b> ; Recorded event code. This parameter is the interface to a FIFO, which contains a total of <b>ERCOUNT</b> recorded event codes. <b>ERCODE</b> belongs to the <b>ERTIME</b> in the Event Recorder Time Register, so must be read together with <b>ERCODE</b> When <b>ERCOUNT</b> equals 0 the value of <b>ERCODE</b> is invalid.	R	0
31:7	Reserved	R	0

## 2.1.10 Event Recorder Time Register (0x07C)

Bit	Description	R/W	Reset
31:0	<b>ERTIME</b> ; Number of counted clock cycles since received start timing event code <b>EREVENT</b> . At which an event has been recorded. This parameter is the interface to a FIFO, which contains a total of <b>ERCOUNT</b> recorded event code times. <b>ERTIME</b> belongs to the <b>ERCODE</b> in the Event Recorder Code Register, so must be read together with <b>ERCODE</b> . When <b>ERCOUNT</b> equals 0 the value of <b>ERTIME</b> is invalid.	R	0

## 2.1.11 Event Code Registers, 1 to 16 (0x080-0x0BC)

Bit	Description	R/W	Reset
6:0	<b>ECEVENT</b> ; Timing event code, which should be recognized and used. Event code 0x00 will be ignored when received from the timing highway, so will not have effect on the event code recognition. However when event code 0x00 is given using an <b>EVENT</b> command the event code is recognized. Event code 0x00 can be transmitted over the timing highway when <b>ECDIR</b> is set to transmit.	R/W	0
14:7	<b>ECCHEN</b> ; Timing channel enable. The channels (1 to 8), which must receive a timing event trigger after receiving the timing event specified in <b>ECEVENT</b> . The least significant bit of <b>ECCHEN</b> indicates timing channel 1 and the most significant bit indicates timing channel 8. <i>This parameter only applies to the Event Code Receive mode.</i>	R/W	0
16:15	<b>ECTIMEEV</b> ; Trigger (Timing Event) type sent to the timing channel counters after receiving the specified event code. 00 = General purpose timing event trigger. 01 = Start timing event trigger. When the timer channel is already started this event is not used. 10 = Stop timing event trigger. When the timer channel is not started this event is not used. 11 = Reserved <i>This parameter only applies to the Event Code Receive mode.</i>	R/W	0
17	<b>ECDIR</b> ; Selection of the event code use. 0 = Receive (Decode). Use <b>ECEVENT</b> to trigger timing channels. 1 = Transmit (Encode) the <b>ECEVENT</b> event code after receiving a trigger. <b>ECCHEN</b> , <b>ECSTART</b> and <b>ECSTOP</b> are ignored.	R/W	0
18	<b>ECTRIGEDGE</b> ; Selection of the active edge of the trigger signal 0 = Rising edge. 1 = Falling edge. <i>This parameter only applies to the Event Code Transmit mode.</i>	R/W	0
20:19	<b>ECTRIGSRC</b> ; Source of the trigger when <b>ECDIR</b> is set to Transmit. The event code is transmitted after receiving a trigger on one of the following signals. 00 = PXI star trigger input. 01 = Front/Rear: Use the signal of a front or rear input. 10 = PXI trigger input. 11 = Reserved <i>This parameter only applies to the Event Code Transmit mode.</i>	R/W	0
24:21	<b>ECTRIGCH</b> ; Selection of the channel when <b>ECTRIGSRC</b> is not set to 00 (= PXI start trigger input). When <b>ECTRIGSRC</b> is set to 10 (=PXI trigger input) the most significant bit of <b>ECGATECH</b> is ignored. <i>This parameter only applies to the Event Code Transmit mode.</i>	R/W	0
31:25	Reserved	R	0

When both **ECSTART** and **ECSTOP** are selected the two bits are cleared and the timing event remains active as a non-explicit start or stop timing event.

ECTRIGSRC	ECTRIGCH	Description
00	XXXX	PXI star trigger input
01	0000 – 1111	Front panel digital I/O channel 1 to 16
10	0000 – 0111	PXI trigger input 0 to 7
10	1000 – 1111	PXI trigger input 0 to 7
11	XXXX	Reserved

**Note:** Transmit is enabled using **ECDIR**. Receive is enabled through **ECCHEN**.

## 2.1.12 Timing Channel Mode Registers, channel 1 to 8

Bit	Description	R/W	Reset
1:0	<b>TCTRIG</b> ; Selection of the external source of the trigger signal 00 = Trigger disabled 01 = I/O trigger (rising edge). Through Front, Rear or PXI. 10 = I/O trigger (falling edge). Through Front, Rear or PXI. 11 = Timing event. Through optical input or software command. A software TRIG command remains always available.	R/W	0
3:2	<b>TCTRIGSRC</b> ; Source of the trigger when TCTRIG is an I/O trigger (001 or 010). 00 = PXI star trigger input. 01 = Front/Rear: Use the signal of a front or rear input. 10 = PXI trigger input. 11 = Reserved	R/W	0
7:4	<b>TCTRIGCH</b> ; Selection of the channel when <b>TCTRIGSRC</b> is not set to 00 (= PXI start trigger input). When <b>TCTRIGSRC</b> is set to 10 (=PXI trigger input) the most significant bit of <b>TCGATECH</b> is ignored.	R/W	0
9:8	<b>TCGATE</b> ; Selection of the external source of the gate signal 00 = Gate disabled 01 = I/O gate (low level). Through Front, Rear or PXI. 10 = I/O gate (high level). Through Front, Rear or PXI. 11 = Reserved. A software GATEON or GATEOFF command remains always available. Since the external gate source is OR-ed with the GATEON/GATEOFF command the timing channel must be placed in the GATEOFF mode to enable the use of the external gate.	R/W	0
11:10	<b>TCGATESRC</b> ; Source of the gate when TCGATE is an I/O gate (01 or 10). 00 = PXI star trigger input. 01 = Front/Rear: Use the signal of a front or rear input. 10 = PXI trigger input. 11 = Reserved	R/W	0
15:12	<b>TCGATECH</b> ; Selection of the channel when <b>TCGATESRC</b> is not set to 00 (= PXI start trigger input). When <b>TCGATESRC</b> is set to 10 (=PXI trigger input) the most significant bit of <b>TCGATECH</b> is ignored.	R/W	0
16	<b>TCGATESYNC</b> ; When set the gate signal is synchronized to the end of a cycle part. So to the end of part 1 or 2 of a cycle in phase 1 or 2. 0 = Asynchronous gate 1 = Synchronous gate	R/W	0
17	<b>TCCYCLIC</b> ; When set, indicates that the channel is ready to receive a new trigger with is has switched back to Phase 1.	R/W	0
18	<b>TCTERM2</b> ; When set, terminates Phase 2 after receiving a trigger. When this bit is set the Phase 2 Duration Register value is not used.	R/W	0
19	<b>TCIDLELEV</b> ; The default output level of the timing channel when the DIO2 is disarmed (IDLE) or when the output during phase 1 or 2 is not driven by one of the cycle part counters.	R/W	0
20	<b>TCINTEN</b> ; Enable PCI interrupt generation after receiving a trigger, which affected the timing channel.	R/W	0
21	<b>PH1CYC1LEV</b> ; The phase 1 starting level. The output level of cycle part 1 of phase 1. This is the output level with which phase 1 output starts. Default this is high and so the next level of the output will be low. With this it is possible to select an inverted or non-inverted signal.	R/W	1
22	<b>PH1CYC2LEV</b> ; The level of phase 1, cycle part 2. This is the output level of the last part of a clock cycle generated within phase 1.	R/W	0
23	<b>PH2CYC1LEV</b> ; The phase 2 starting level. The output level of cycle part 1 of phase 2. This is the output level with which phase 2 output starts.	R/W	1
24	<b>PH2CYC2LEV</b> ; The level of phase 2, cycle part 2. This is the output level of the last part of a clock cycle generated within phase 2.	R/W	0
31:25	Reserved	R	0

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TCTRIGSRC / TCGATESRC	TCTRIGCH	Description
00	XXXX	PXI star trigger input
01	0000 – 1111	Front panel digital I/O channel 1 to 16
10	0000 – 0111	PXI trigger input 0 to 7
10	1000 – 1111	PXI trigger input 0 to 7
11	XXXX	Reserved

**Note:** Changing the contents of the Timing Channel Mode Register can only be done when the timing channel is in the IDLE state.

### 2.1.13 Phase 1 Cycle Part 1 Registers, channel 1 to 8

Bit	Description	R/W	Reset
31:0	<b>PH1CYCLE1;</b> The number of counted clock cycles + 1, which the first part of an output cycle in phase 1, must last. The output level is defined with <b>PH1CYC1LEV</b> . <i>This register will not be cleared after a reset (Reset Register).</i>	R/W	X

### 2.1.14 Phase 1 Cycle Part 2 Registers, channel 1 to 8

Bit	Description	R/W	Reset
31:0	<b>PH1CYCLE2;</b> The number of counted clock cycles + 1, which the second part of an output cycle in phase 1, must last. The output level is defined with <b>PH1CYC2LEV</b> . <i>This register will not be cleared after a reset (Reset Register).</i>	R/W	X

### 2.1.15 Phase 2 Cycle Part 1 Registers, channel 1 to 8

Bit	Description	R/W	Reset
31:0	<b>PH2CYCLE1;</b> The number of counted clock cycles + 1, which the first part of an output cycle in phase 2, must last. The output level is defined with <b>PH2CYC1LEV</b> . <i>This register will not be cleared after a reset (Reset Register).</i>	R/W	X

### 2.1.16 Phase 2 Cycle Part 2 Registers, channel 1 to 8

Bit	Description	R/W	Reset
31:0	<b>PH2CYCLE2;</b> The number of counted clock cycles + 1, which the second part of an output cycle in phase 2, must last. The output level is defined with <b>PH2CYC2LEV</b> . <i>This register will not be cleared after a reset (Reset Register).</i>	R/W	X

## 2.1.17 Phase 2 Delay Registers, channel 1 to 8

Bit	Description	R/W	Reset
31:0	<b>PH2DELAY</b> ; The number of counted clock cycles + 1, which the delay between the trigger recognition and the switch from phase 1 to phase 2 must last. The output remains working in phase 1 until the switch over. <i>This register will not be cleared after a reset (Reset Register).</i>	R/W	X

## 2.1.18 Phase 2 Duration Registers, channel 1 to 8

Bit	Description	R/W	Reset
31:0	<b>PH2DUR</b> ; The number of counted clock cycles + 1, which phase 2 lasts until it is automatically terminated. Only used when <b>TCTERM2</b> is not set. <i>This register will not be cleared after a reset (Reset Register).</i>	R/W	X

## 2.1.19 Phase 1 Counter Status Registers, channel 1 to 8

Bit	Description	R/W	Reset
31:0	<b>PH1COUNT</b> ; The number of counted timing channel clock cycles which phase 1 is currently active or lasted. The counter is cleared when the timing channel is armed. The counter value starts (at 0) when the timing channel is started, and stops when the timing channel has switched to phase 2. The counter will not continue when the timing channel switches back to phase 1. So only the first phase 1, after arming the timing channel, will be counted. <i>This register will not be cleared after a reset (Reset Register). It will be cleared when the timing channel is in the Armed state.</i>	R	X

## 2.1.20 Phase 2 Counter Status Registers, channel 1 to 8

Bit	Description	R/W	Reset
31:0	<b>PH2COUNT</b> ; The number of counted timing channel clock cycles which phase 2 is currently active or lasted. The counter is cleared when the timing channel is armed. It starts counting when phase 2 has been entered and stops when phase 2 terminates. Only the first phase 2, after arming the timing channel, will be counted. <i>This register will not be cleared after a reset (Reset Register). It will be cleared when the timing channel is in the Armed state.</i>	R	X

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## 2.1.21 Timing Channel Status Register 1 (0x2C0-2FC)

Bit	Description	R/W	Reset
7:0	<b>TCLEVEL</b> ; The timing channel's current output level. The least significant bit of <b>TCLEVEL</b> indicates the current level for timing channel 1. The most significant bit indicates the current output level for timing channel 8.	R	0
15:8	<b>TCTRIGGERED</b> ; These bits are set when the timing channel has been triggered. These bits are cleared when the DIO2 is Disarmed.	R	0
23:16	<b>TCINT</b> ; PCI interrupt event has been generated after receiving a trigger, which affected the timing channel. The least significant bit of <b>TCINT</b> indicates an interrupt for timing channel 1. The most significant bit indicates an interrupt for timing channel 8.	R	0
31:24	Reserved	R	0

## 2.1.22 Timing Channel Status Register 2 (0x300-3FC)

Bit	Description	R/W	Reset
1:0	<b>TCSTATUS1</b> ; The timing channel 1 current status.	R	0
3:2	<b>TCSTATUS2</b> ; The timing channel 2 current status.	R	0
5:4	<b>TCSTATUS3</b> ; The timing channel 3 current status.	R	0
7:6	<b>TCSTATUS4</b> ; The timing channel 4 current status.	R	0
9:8	<b>TCSTATUS5</b> ; The timing channel 5 current status.	R	0
11:10	<b>TCSTATUS6</b> ; The timing channel 6 current status.	R	0
13:12	<b>TCSTATUS7</b> ; The timing channel 7 current status.	R	0
15:14	<b>TCSTATUS8</b> ; The timing channel 8 current status.	R	0
31:16	Reserved	R	0

TCSTATUSx	Description
00	<b>IDLE</b> ; The timing channel is doing nothing. It has been DISARMed.
01	<b>ARMED</b> ; The timing channel has been ARMED and is waiting for a start trigger/event or START command.
10	<b>PHASE1</b> ; The timing channel is active in phase 1.
11	<b>PHASE2</b> ; The timing channel is active in phase 2.

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## 2.2 CompactPCI interface

### 2.2.1 Mechanical

The CompactPCI interface is provided using the standard Hard Metric 2mm type A connector. This connector (J1) is available at the rear side of the board.

### 2.2.2 Electrical

The CompactPCI interface is implemented using a PLX PCI9054 PCI Controller. This controller is compliant to the "PCI Local Bus Specification, Revision 2.2".

- |            |                                |
|------------|--------------------------------|
| • DC Power | 5 Volt and 3.3 Volt through J1 |
|------------|--------------------------------|

### 2.2.3 Functional

The CompactPCI interface is implemented compliant to "PCI Local Bus Specification, Revision 2.2" and "PICMG 2.0 R3.0 CompactPCI Specification".

The interface has the following features and characteristics.

- |                           |   |
|---------------------------|---|
| • Bus width               | 32 bit  |
| • Clock                   | 33 MHz  |
| • Configuration           | Target (Slave)  |
| • Interrupt               | INTA# generated on: <ul style="list-style-type: none"><li>• Timing channel received trigger</li><li>• Event Recorder FIFO half full</li><li>• Front I/O error detection</li></ul> |
| • Hot swap                | No  |
| • Geographical addressing | No  |

### 2.2.4 Allocation

The CompactPCI interface is completely implemented through connector J1. CompactPCI specific signals through J2 are not used.

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## 2.3 PXI interface

### 2.3.1 Mechanical

The PXI interface is provided using the standard Hard Metric 2mm type B connector. This connector (J2) is available at the rear side of the board.

### 2.3.2 Electrical

The PXI interface is implemented compliant to the "PXI Specification, Revision 2.0"

### 2.3.3 Functional

The PXI interface is implemented compliant to "PXI Specification, Revision 2.0". Not all features of the PXI standard are available. Only the following can be used.

- Trigger input: PXI Star Trigger (**PXI\_STAR**) and the PXI Trigger bus signals (**PXI\_TRIG[7:0]**).
- Timing output: The PXI Trigger bus signals (**PXI\_TRIG[7:0]**).
- Clock output: The most significant PXI Trigger bus signals (**PXI\_TRIG7**). This output is capable if creating a clean clock signal.

When **PXI\_TRIG7** is used for the timing channel clock generation (See Clock Control Register) the frequency must not exceed 40MHz.

The trigger signals cannot be synchronized to the **PXI\_CLK10**. The **PXI\_CLK10** signal is not used.

### 2.3.4 Allocation

The PXI interface is implemented through connector J2. CompactPCI specific signals through J2 are not used.

## 2.4 Front panel digital in/out

### 2.4.1 Mechanical

The I/O interfaces are provided using 16 coaxial (uni-pole) connectors, type EPL.00.250.NTN from LEMO. These connectors are available through the front panel.

### 2.4.2 Electrical

The I/O interface can be configured as **INPUT** or **OUTPUT**. When the output is not used the input can have a selectable line termination of 50Ω. The output is capable of driving a 50Ω cable with termination.

#### Input characteristics

• High-level input voltage (min)	2V
• Low-level input voltage (max)	0.8V
• Input voltage	-2V (clamped at -0.3) to 7V
• Input threshold level	± 1.4V with 0.4V hysteresis
• Input impedance	± 5kΩ
• Line termination	50Ω (selectable)

#### Output characteristics

• High-level output voltage (min)	4.8V (no line termination) 2.4V (with 50Ω line termination)
• Low-level output voltage (max)	0.4V
• Output current	50mA (with 50Ω line termination)
• Output short-circuit current	140mA (max)
• Short-circuit duration	Continuous
• Short-circuit to voltage level	-2V to 7V

**Note:** The output is always read back through the input. When the input signal level (high or low) is not equal to the driven output signal level, the output will be put in a high impedance state. A front panel LED and a status bit indicate this. An interrupt can be generated.

**Note:** This I/O error detection works up to a driving frequency of above 5MHz (the maximum Timing Channel output frequency), when short circuited to 0V. Output signals with a frequency above 5 to 7MHz will not trigger the short circuit detection. When a short circuit is made to another voltage level than 0V, the I/O error detection can work up to a

frequency below 5MHz. This frequency depends on parameters like the short circuit voltage level, the maximum current drive and output resistance of the short circuiting output driver.

### 2.4.3 Functional

The I/O interface can have different logical functions, which are defined in the FPGA of the DIO2.

As stated before, the output is monitored through the input to detect possible short circuit situations. When such a situation has been detected the output is placed in it's high impedance state until the problem has been resolved and this I/O error is cleared. Clearing the I/O error can be done through a CompactPCI addressable register.

When a front I/O is used for the timing channel clock generation (See Clock Control Register) the frequency must not exceed 10MHz.

### 2.4.4 Allocation

The I/O interfaces can be accessed using a LEMO series 00 connector located in the front panel of the DIO2.

Next to each I/O interface connector there is a LED, which indicate the following statuses.

LED	In/Out	Status
Off	-	I/O disabled (Rear side selected), Power off or FPGA not configured
Green	In	Input selected (Green = Everything OK)
Yellow/Orange	Out	Output selected (Yellow = Attention, this is a output)
Red	In (Out in 3-State)	Short circuit detected (Red = Error)

## 2.5 Rear panel digital in/out

### 2.5.1 Mechanical

The Rear I/O interface is provided using the standard Hard Metric 2mm type B connector. This connector (J5) is available at the rear side of the board.

### 2.5.2 Electrical

The Rear I/O interface consists of several signals.

Provided are the CompactPCI +5V and +3.3V for use by the Transition module. These are power supply outputs.

The separate +5V power supply for the Optical I/O can be provided here. This is a power supply input.

The 16 digital rear I/O signals have the following characteristics:

#### Input characteristics

• High-level input voltage (min)	2V
• Low-level input voltage (max)	0.8V
• Input voltage	-0.5V to 5.5V
• Input clamp current	-50mA

#### Output characteristics

• High-level output voltage (min)	4.8V
• Low-level output voltage (max)	0.4V
• Output type	Open collector with 1k $\Omega$ pull-up to +5V.

#### Power characteristics

• DC Power	5 Volt through J5
• Current	70mA (typ)

### 2.5.3 Functional

The Rear I/O interface can have different logical functions, which are defined in the FPGA of the DIO2.



When a rear I/O is used for the timing channel clock generation (See Clock Control Register) the frequency must not exceed 20MHz.

## 2.5.4 Allocation

The Rear I/O is implemented so it does not become incompatible with the following standards.

- VITA 29.1(PC•MIP Pin Mapping to CompactPCI and VME64X)
- PICMG 2.3 (PMC I/O Pin Assignments on CompactPCI)
- PICMG 2.4 (IP I/O Pin Assignments on CompactPCI)

These standards could be used by different Transition Modules to interface with CompactPCI modules. In all three cases the Rear I/O signals and the Optical I/O power supply can be accessed as if there was a PC•MIP, PMC or IndustryPack module attached in the DIO2.

The interface is implemented through connector J5 only. For VITA 29.1 only the PC•MIP-U is available. For PICMG 2.3 only the I/O pins 1 to 55 are connected and defined. For PICMG 2.4 only Slot D is available.

Pin	Row A	Row B	Row C	Row D	Row E	Row F	Compliance		
22	+3.3V	+3.3V	+3.3V	+5V	+5V	GND	PC•MIP-U	IndustryPack Slot D	PMC I/O 1 to 64
21	GND	GND	GND	OPTO +5V	OPTO +5V	GND			
20	GND	GND	GND	REAR 1	REAR 2	GND			
19	GND	GND	GND	REAR 3	REAR 4	GND			
18	GND	GND	GND	REAR 5	REAR 6	GND			
17	GND	GND	GND	REAR 6	REAR 8	GND			
16	GND	GND	GND	REAR 9	REAR 10	GND			
15	GND	GND	GND	REAR 11	REAR 12	GND			
14	GND	GND	GND	REAR 13	REAR 14	GND			
13	GND	GND	GND	REAR 15	REAR 16	GND			
12	+3.3V	+3.3V	+3.3V	+5V	+5V	GND			
11	n.c.	n.c.	n.c.	n.c.	n.c.	GND			
10	n.c.	n.c.	n.c.	n.c.	n.c.	GND			
9	n.c.	n.c.	n.c.	n.c.	n.c.	GND			
:	n.c.	n.c.	n.c.	n.c.	n.c.	GND			
1	n.c.	n.c.	n.c.	n.c.	n.c.	GND			

Signal	Pin PC•MIP-U	Pin IndustryPack Slot D	Pin PMC I/O
REAR 1	11	14	12
REAR 2	12	15	11
REAR 3	17	19	17
REAR 4	19	20	16
REAR 5	24	24	22
REAR 6	25	25	21
REAR 7	31	29	27
REAR 8	32	30	26
REAR 9	38	34	32
REAR 10	39	35	31
REAR 11	44	39	37

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Signal	Pin PC•MIP-U	Pin IndustryPack Slot D	Pin PMC I/O
REAR 12	46	40	36
REAR 13	51	44	42
REAR 14	52	45	41
REAR 15	57	49	47
REAR 16	59	50	46
+5V	63-64	4-5	1-2, 51-52
+3.3V	60-62	1-3	3-5, 53-55
OPTO +5V	4, 6	9-10	6-7
GND	1-3, 7-9, 14-16, 20, 22-23, 27-28, 30, 33, 35-36, 40-41, 43, 47-49, 54-56	6-8, 11-13, 16-18, 21-23, 26-28, 31-33, 36-38, 41-43, 46-48	8-10, 13-15, 18-20, 23-25, 28-30, 33-35, 38-40, 43-45, 48-50
n.c.			56-64

## 2.6 Optical In/Out

### 2.6.1 Mechanical

The Optical I/O interface is provided using two ST optical connectors. These connectors are available through the front panel.

### 2.6.2 Optical/Electrical

The Optical I/O interface has one **INPUT** and one **OUTPUT**. The input is implemented using an HFPR-2416 Optical Receiver, and the output is implemented using an HFPR-1414 Optical Transmitter, both from Agilent. For detailed characteristics see the datasheets of these devices.

Both devices operate best with light with a wave length of 820nm, using a 62.5/125 mm multimode glass fiber cable.

### 2.6.3 Logical

The Optical I/O interface can be used in different modes.

- The optical input can be used as the source for the Timing Highway.
- The optical output can have it's source from the optical input directly. This can be selected during operational mode or is automatically selected when the CompactPCI power is turned off. This automatic bypass mode is only available when a separate power supply (+5V) is provided through J5.
- The optical output can also be a signal generated from within the FPGA.

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## 2.6.4 Allocation

The Optical I/O interfaces can be accessed using two ST connectors. These two connectors will be available through the front panel and located at the top of the front panel.

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## 2.7 LED User Interface

### 2.7.1 Function

There are two groups of LEDs to give information to the user. The first group consists of the three color LEDs which indicate the I/O status of the front panel digital I/Os.

I/O Status LED	Digital In/Out	Status
Off	-	I/O disabled (Rear side selected), Power off or FPGA not configured
Green	In	Input selected (Green = Everything OK)
Yellow/Orange	Out	Output selected (Yellow = Attention, this is a output)
Red	In (Out in 3-State)	Short circuit detected (Red = Error)

The other group of LEDs are used to indicate the functional mode of the DIO2. All three LEDs are yellow.

Function LED	Description
Clock OK	Optical clock is present
Event	Event has been received
Backup +5V OK	OPTO +5V backup power is present

### 2.7.2 Allocation

The I/O status LEDs are located in the front panel, next to the LEMO connectors. One next to each front panel digital I/O interface.

The function LEDs are also located in the front panel, at the top of the front panel.

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