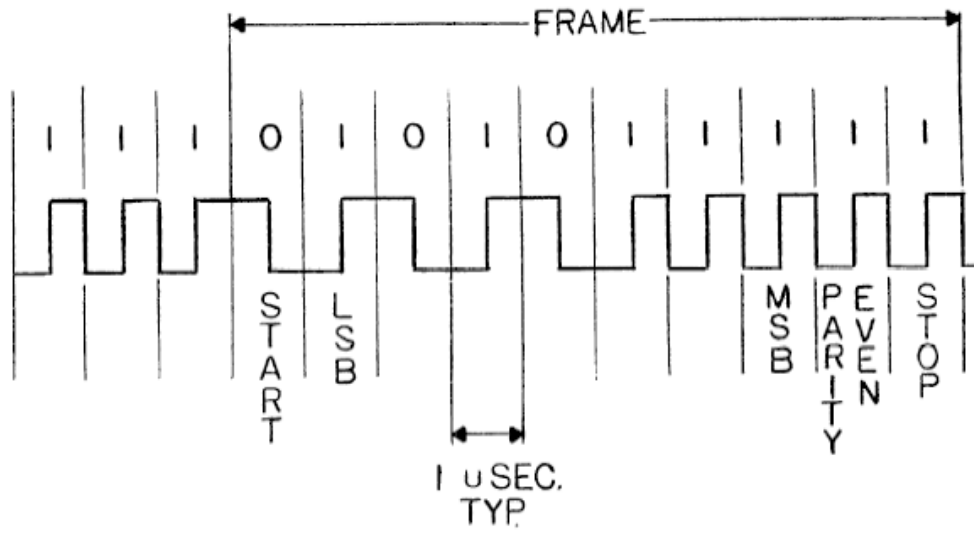


PPPL Clock Link Timing Waveform
20October2003



INCAA DIO2 Timing Highway Waveform

2003-09-12

Signal, which, because it is bi-phase encoded, results in a clock of 1MHz when no data is received. A rising edge within the middle of a 1µs period represents a logical '0' and a falling edge a logical '1'. During idle state a logical '1' is bi-phase encoded. When data is received this will be a timing event which can be used as a trigger of the timing channels. The received event can also be recorded in a 32 events deep FIFO including a time stamp.

The DIO2 is also capable of encoding and transmitting timing highway events. A software command or a selected trigger can cause the transmission of a timing event.

The encoded timing highway signal starts with a start bit (logical '0'), followed by 7 data bits (LSB first), a even parity bit and a stop bit (logical '1'). Because 1 bit lasts 1µs the transmission of a timing event takes 10µs.

An example of the timing highway signal can be seen below.

The diagram shows a timing event of 10µs duration. The signal is bi-phase encoded, with a rising edge representing a logical '0' and a falling edge representing a logical '1'. The waveform starts with a start bit (logical '0'), followed by 7 data bits (LSB first), a even parity bit, and a stop bit (logical '1'). The bits are: 1 1 1 0 1 1 0 1 0 0 0 1 1 1 1. The signal is labeled as 'Light' and 'Dark'.

The 1MHz clock which is encoded in the signal at all times is decoded out of the timing highway signal and can be used (multiplied by 10) to clock the timing channels with.