DIO2
Digital I/O (Timing Module)

Hardware Design Description Documentation

CP-DIO2-5023

0 TABLE OF CONTENTS

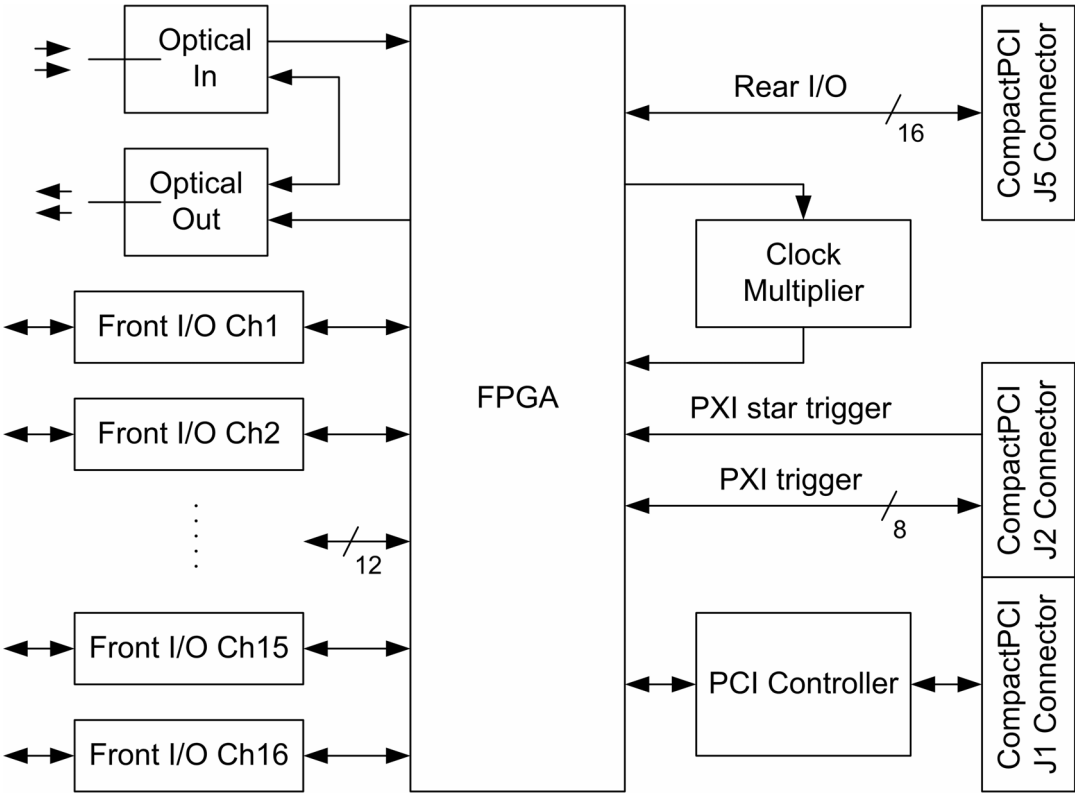
REVISION HISTORY

Date	Rev.	Prep. by	Comment
2002-05-13	A	REB	• Initial draft version.
2002-05-30	A	REB	• Changed command code of several commands. • Added **TCGATESYNC** to Timing Channel Mode Register. • Changed description of the Phase x Cycle Part x Registers.
2002-05-31	A	REB	• Added **BUSY** bit to the General Status Register. • Changed **TCSCLRON** bits to **TCSTARTED** bits. • Removed **STATE** parameter from the General Status Register.
2002-06-03	A	REB	• Changed description of the Phase x Counter Status Registers. • Added Event Recorder Register, Event Recorder Code Register and Event Recorder Time Register. • Added commands in the General Control Register for Event Recorder control.
2002-06-07	A	REB	• Added description of the **TCGATE** parameter. • Address map assignments made. • Updated timing channel state diagram. • Updated DIO2 block diagram. • Added timing channel clock limitation with an external clock. • Changed synchronization clock (timing clock) description.
2002-06-11	A	REB	• Added **CLKOK** status bit to the Clock Control Register. • Added interrupt generation on Event Recorder FIFO half full.
2002-06-12	A	REB	• Removed **TCSTARTED** bits from Timing Channel Status Register 1 since this information is also in the Timing Channel Status Register 2 under the **TCSTATUS** bits.
2002-06-18	A	REB	• Removed **OPTOTXEN** bit from the General Control Register. • Changed bit positions within General Control Register.
2002-06-20	A	REB	• Updated the Note with the Clock Control Register regarding the reset. • Corrected **CLKSRC** parameter description • Updated EVENT command description. • Updated description of **IO50OHM** parameter.
2002-06-27	A	REB	• Changed timing channel clock limitations with an external clock. The clock frequency must now be four times the desired timing channel frequency.
2002-06-28	A	REB	• Added I/O error interrupt in General Status Register and I/O Connection Registers.
2002-08-06	A	REB	• Changed the Event Recorder size from 64 to 32. • Changed the Event Recorder Register: **ERCOUNT** is now 6 bits wide and **ERINTEN** is now located at bit 15.
2002-10-02	A	REB	• Added STOP command in General Control Register. • Changed **ECSTART** and **ECSTOP** bits to **ECTIMEEV** parameter in Event Code Register.
2002-11-01	A	REB	• Added description of the timing channels and the timing highway.

Date	Rev.	Prep. by	Comment
2002-11-21	A	REB	• Added description about power up situation of timing highway decoder.
2003-01-03	A	REB	• Added notes to **ECEVENT** in the Event Code Register. • Added **CLKTHSYNC** and **CLKTHOUT** parameters to the Clock Control Register.
2003-02-17	A	REB	• Added component allocation picture.
2003-05-19	A	REB	• Added some pictures for clarification of the DIO2 features.

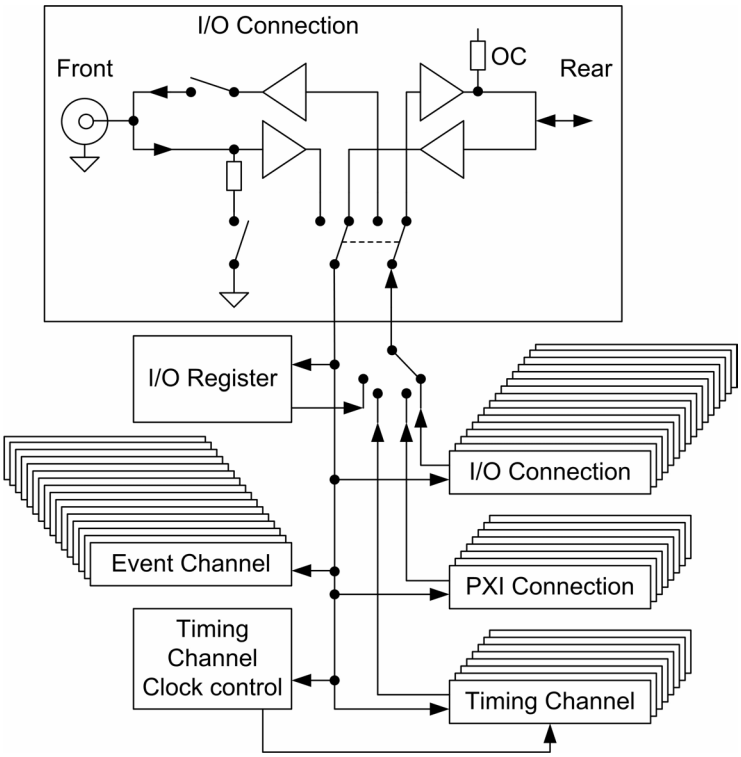
1 FUNCTIONAL/LOGICAL DESCRIPTION

The DIO2 is a general purpose, 16 channel, digital I/O module with 8 flexible assignable timing/trigger channels in a 6U high CompactPCI form factor. The 16 channels can be used via the front panel or the rear side.
The timing channels can be assigned to any of the 16 front or rear side I/Os or to any of the PXI trigger signals. They are synchronized to an external or internal clock.



1.1 Front and rear digital I/O

The digital I/O channels can work in different modes. The ‘normal’ transparent mode provides register based direct I/O. In a few different ‘buffer’ modes, selected signals can be buffered to other outputs to provide, for example, a star trigger or timing geometry. And there is the ‘timing’ mode in which, a selected (one of eight) timing channels can be assigned to one or more outputs.
The DIO2 is a 16 channel digital I/O module and therefore each channel can have it’s source and destination on the front or the rear side of the module. When the front is selected the rear side is ignored and vice versa.



1.1.1 Front panel

The front digital output is capable of driving a 50Ω load. When needed a 50Ω input termination can be selected. This input termination can be switched on or off by register access.

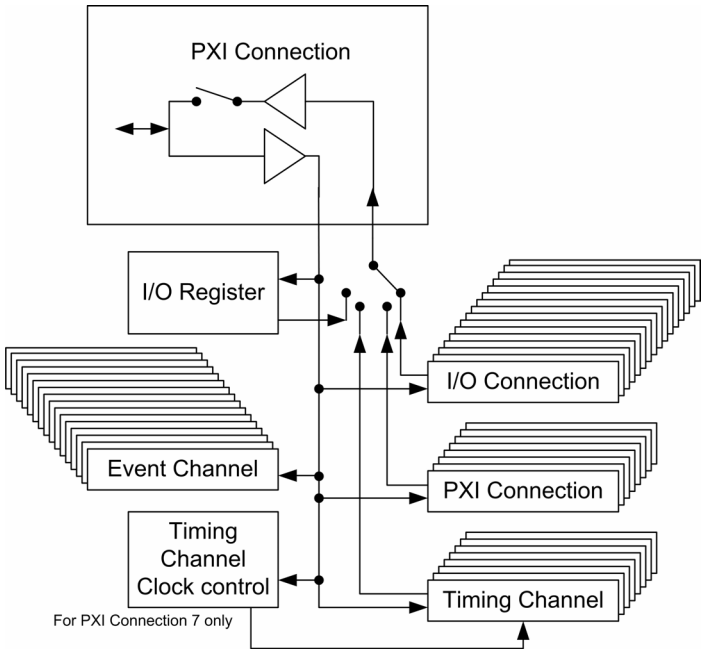
Since the I/O buffer circuit can be used as an input and an output, an extra protection has been build in. When the clock buffer is set to be an output, the input is read back and compared to the driven level. When these are not equal the output is disabled and an error is indicated through a front LED, a status bit and/or an interrupt.

1.1.2 Rear side

There are digital inputs and output on the rear side of the module. The rear digital output is an open-collector output with a 10kΩ pull-up. In this way it can be used on a transition module without problems. It can even be bussed up to 8 loads (when all have a 10kΩ pull-up). These outputs are not capable of driving a cable of any sort. A transition module mounted on the rear side of CompactPCI, should provide appropriate cable drivers when needed.
The inputs are 5V tolerant and are always enabled.

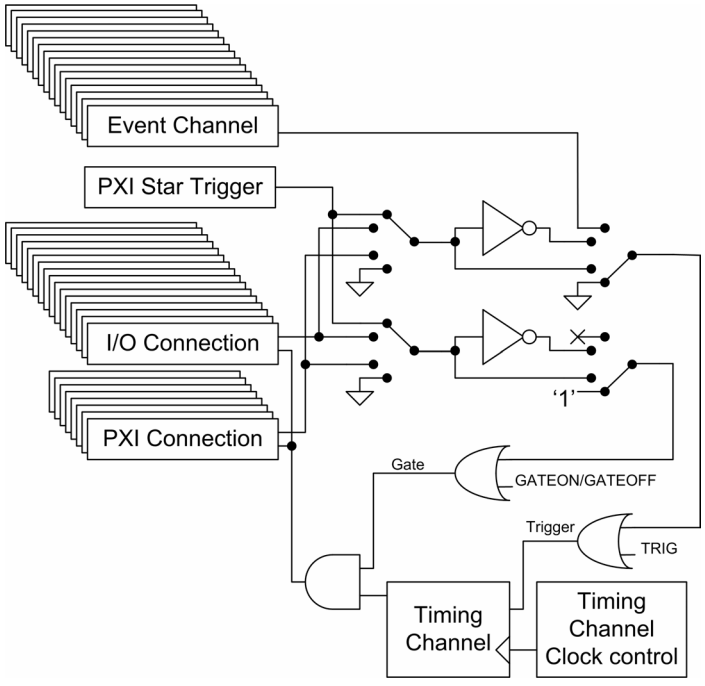
1.2 PXI triggers and timing

The PXI interface consists of 8 PXI trigger signals and one PXI star trigger input. PXI trigger signals can be defined as input or output and can work in different modes also. The 'normal' transparent mode provides register based direct I/O. Two 'buffer' modes are available where selected front or rear signals can be buffered to the PXI triggers. And there is the 'timing' mode in which, a selected (one of eight) timing channel can be assigned to one or more PXI trigger outputs. One PXI trigger signal (**PXI_TRIG7**) is especially designed to transport a clock to other modules.



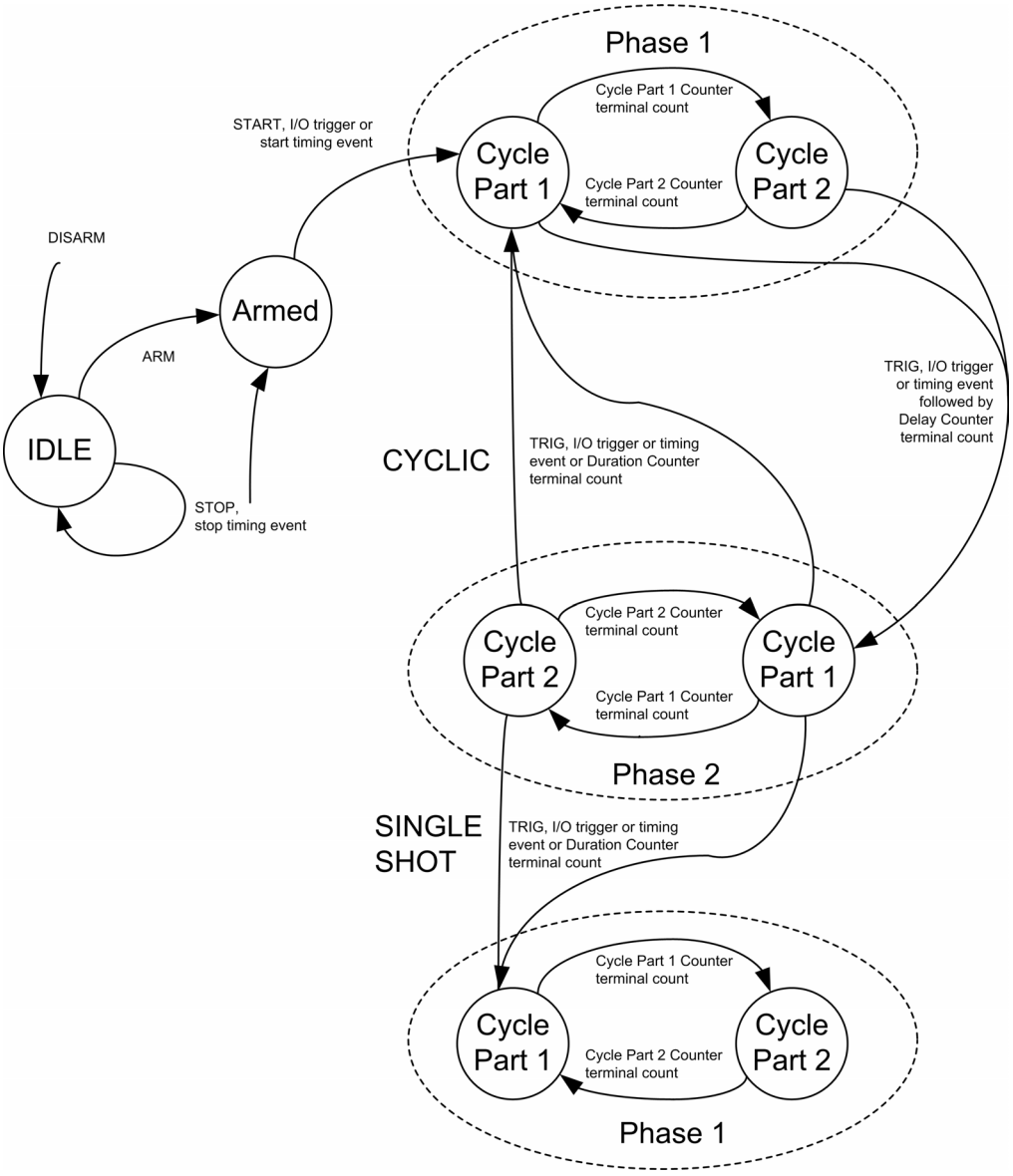
1.3 Timing channels

The 8 different timing channels can be assigned to one or more digital I/Os (front and/or rear) or one or more PXI trigger signals.
The 8 timing channels have a multiple phase configuration. The change from one phase to the next can be controlled using different triggers, which can be selected per timing channel. Triggers like: software trigger, front/rear I/O and PXI trigger, and the PXI star trigger are available. A timing event, received via the optical input can also be used as a trigger for the timing channel.
The timing channels can also be gated. This gate can be a software gate, a front/rear I/O and PXI trigger signal, or the PXI star trigger signal.



1.3.1 Timing phases

The timing channels have two phases. During each phase a periodic signal can be generated. This periodic signal consist of two cycle parts of which the duration and the output level can be defined. So it is possible to create clock signals, DC levels and pulses.



When the timing channel has been armed it can be started using a START command, a trigger or a timing event (general or start). The timing channel always starts in Phase 1. The output signals alternates between the levels of cycle part 1 and cycle part 2 until the timing channel changes over to Phase 2.

This change over will take place after a trigger and a specified delay (which can be 0). During Phase 2 the output signals alternates between the levels of cycle part 1 and cycle part 2 of phase 2. A Change over from Phase 2 back to Phase 1 can occur after another trigger or after a specified duration.
When the timing channel is in cyclic mode it can be retriggered to change over to Phase 2 again. In non-cyclic mode (single shot) the timing channel will remain in Phase 1 and can not be retriggered.

1.3.2 Synchronization Clock

The timing channels will operate synchronously to a selected clock. This can be an internal 40MHz clock, an externally provided clock (through PXI, front or rear I/O) or though the optical Timing highway. The Timing high way clock is (normally) 1MHz and is multiplied onboard to the required 40MHz. The timing channels output are timed on a 10MHz clock, which is the mentioned 40MHz divided by four. When an external clock is used (PXI, front or rear I/O) the clock must be four times the needed clock.
The external clock frequency may not be higher than 40MHz or 20MHz depending on the selected clock.

1.4 Connection matrix

As stated before the front, rear and PXI I/O can work in different modes by which connection between different functional parts of the DIO2 can be made.

From \ To	Register	Front/Rear Out ch. 1 to 16	PXI trigger 0 to 7	Trigger Timing ch. 1 to 8	Gate Timing ch. 1 to 8
Register	Via I/O	✓	✓		
Front/Rear In ch. 1 to 16	✓	✓	✓	✓	✓
PXI trigger 0 to 7	✓	✓		✓	✓
PXI star trigger				✓	✓
Trigger Timing ch. 1 to 8	✓	✓	✓	Via I/O	Via I/O
TRIG command				✓	
GATE command					✓

Note: The timing channels can be gated and/or triggered by other timing channels when the timing channel output is directed via a front, rear or PXI output and input, to another timing channel.

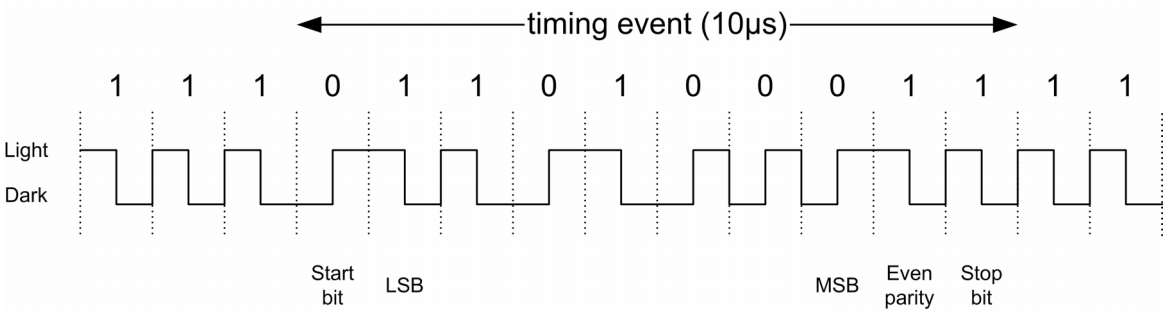
1.5 Timing highway

The timing highway is an optically received, bi-phase encoded (Manchester encoded), signal. Which, because it is bi-phase encoded, results in a clock of 1MHz when no data is received. A rising edge within the middle of a 1µs period represents a logical ‘0’ and a falling edge a logical ‘1’. During idle state a logical ‘1’ is bi-phase encoded.
When data is received this will be a timing events which can be used as a trigger of the timing channels.
The received event can also be recorded in a 32 events deep FIFO including a time stamp.

The DIO2 is also capable of encoding and transmitting timing highway events. A software command or a selected trigger can cause the transmission of a timing event.

The encoded timing highway signal starts with a start bit (logical ‘0’), followed by 7 data bits (LSB first), a even parity bit and a stop bit (logical ‘1’). Because 1 bit lasts 1µs the transmission of a timing event takes 10µs.

An example of the timing highway signal can be seen below.



The 1MHz clock which is encoded in the signal at all times is decoded out of the timing highway signal and can be used (multiplied by 10) to clock the timing channels with.

During power up of the DIO2 it is possible that part of the design which extracts the 1MHz clock out of the timing highway signal locks on the falling edges in the middle of a ‘0’ instead of the falling edges at the start of a ‘1’.
The DIO2 is capable of detecting this situation when valid data is received. To force this, a timing event with an event code 0x00 can be transmitted along the timing highway.

1.6 PCI Controller

The interface with the PCI bus is realized with a PLX 9054 32-bit, 33 MHz PCI bus interface chip. This chip is the interface between the PCI bus and the FPGA. The FPGA is connected to the PCI interface through a local bus. During an access on PCI, the PCI interface chip decides if the local bus should be accessed or not. In case a register is accessed that resides inside the FPGA an access is performed on the local bus. During a write cycle the data is copied from the local bus into the FPGA and during a read cycle the data is copied from the FPGA to the local bus.

2 EXTERNAL INTERFACES

In the tables, within this subsection, the R/W column can contain the following information.

R/W column contents	Description
R/W	Readable and Writable
R	Read only
W	Write only
CR	Clearing Read (clears bit after read)
CW	Clearing Write (bit is cleared right after a write to it)

2.1 PCI Addressable Registers

Address	Description		R/W
0x000	General Control Register		R/W/CW
0x004	General Status Register		R
0x008	Clock Control Register		R/W
0x00C	Version and Reset Register		R/CW
0x010	I/O Connection Register	Channel 1	R/W
0x014	I/O Connection Register	Channel 2	R/W
0x018	I/O Connection Register	Channel 3	R/W
0x01C	I/O Connection Register	Channel 4	R/W
0x020	I/O Connection Register	Channel 5	R/W
0x024	I/O Connection Register	Channel 6	R/W
0x028	I/O Connection Register	Channel 7	R/W
0x02C	I/O Connection Register	Channel 8	R/W
0x030	I/O Connection Register	Channel 9	R/W
0x034	I/O Connection Register	Channel 10	R/W
0x038	I/O Connection Register	Channel 11	R/W
0x03C	I/O Connection Register	Channel 12	R/W
0x040	I/O Connection Register	Channel 13	R/W
0x044	I/O Connection Register	Channel 14	R/W
0x048	I/O Connection Register	Channel 15	R/W
0x04C	I/O Connection Register	Channel 16	R/W
0x050	PXI Connection Register	Trigger 0	R/W
0x054	PXI Connection Register	Trigger 1	R/W
0x058	PXI Connection Register	Trigger 2	R/W
0x05C	PXI Connection Register	Trigger 3	R/W
0x060	PXI Connection Register	Trigger 4	R/W
0x064	PXI Connection Register	Trigger 5	R/W
0x068	PXI Connection Register	Trigger 6	R/W
0x06C	PXI Connection Register	Trigger 7	R/W
0x070	I/O Register		R/W
0x074	Event Recorder Register		R/W
0x078	Event Recorder Code Register		R
0x07C	Event Recorder Time Register		R

Address	Description		R/W
0x080	Event Code Register 1		R/W
0x084	Event Code Register 2		R/W
0x088	Event Code Register 3		R/W
0x08C	Event Code Register 4		R/W
0x090	Event Code Register 5		R/W
0x094	Event Code Register 6		R/W
0x098	Event Code Register 7		R/W
0x09C	Event Code Register 8		R/W
0x0A0	Event Code Register 9		R/W
0x0A4	Event Code Register 10		R/W
0x0A8	Event Code Register 11		R/W
0x0AC	Event Code Register 12		R/W
0x0B0	Event Code Register 13		R/W
0x0B4	Event Code Register 14		R/W
0x0B8	Event Code Register 15		R/W
0x0BC	Event Code Register 16		R/W
0x0C0-0x0DC	Timing Channel Mode Register	Timing Channel 1	R/W
0x0E0	Phase 1 Cycle Part 1 Register		R/W
0x0E4	Phase 1 Cycle Part 2 Register		R/W
0x0E8	Phase 2 Cycle Part 1 Register		R/W
0x0EC	Phase 2 Cycle Part 2 Register		R/W
0x0F0	Phase 2 Delay Register		R/W
0x0F4	Phase 2 Duration Register		R/W
0x0F8	Phase 1 Counter Status		R
0x0FC	Phase 2 Counter Status		R
0x100-0x11C	Timing Channel Mode Register	Timing Channel 2	R/W
0x120	Phase 1 Cycle Part 1 Register		R/W
0x124	Phase 1 Cycle Part 2 Register		R/W
0x128	Phase 2 Cycle Part 1 Register		R/W
0x12C	Phase 2 Cycle Part 2 Register		R/W
0x130	Phase 2 Delay Register		R/W
0x134	Phase 2 Duration Register		R/W
0x138	Phase 1 Counter Status		R
0x13C	Phase 2 Counter Status		R
0x140-0x15C	Timing Channel Mode Register	Timing Channel 3	R/W
0x160	Phase 1 Cycle Part 1 Register		R/W
0x164	Phase 1 Cycle Part 2 Register		R/W
0x168	Phase 2 Cycle Part 1 Register		R/W
0x16C	Phase 2 Cycle Part 2 Register		R/W
0x170	Phase 2 Delay Register		R/W
0x174	Phase 2 Duration Register		R/W
0x178	Phase 1 Counter Status		R
0x17C	Phase 2 Counter Status		R
0x180-0x19C	Timing Channel Mode Register	Timing Channel 4	R/W
0x1A0	Phase 1 Cycle Part 1 Register		R/W
0x1A4	Phase 1 Cycle Part 2 Register		R/W
0x1A8	Phase 2 Cycle Part 1 Register		R/W
0x1AC	Phase 2 Cycle Part 2 Register		R/W
0x1B0	Phase 2 Delay Register		R/W
0x1B4	Phase 2 Duration Register		R/W
0x1B8	Phase 1 Counter Status		R
0x1BC	Phase 2 Counter Status		R

Address	Description		R/W
0x1C0-0x1DC	Timing Channel Mode Register	Timing Channel 5	R/W
0x1E0	Phase 1 Cycle Part 1 Register		R/W
0x1E4	Phase 1 Cycle Part 2 Register		R/W
0x1E8	Phase 2 Cycle Part 1 Register		R/W
0x1EC	Phase 2 Cycle Part 2 Register		R/W
0x1F0	Phase 2 Delay Register		R/W
0x1F4	Phase 2 Duration Register		R/W
0x1F8	Phase 1 Counter Status		R
0x1FC	Phase 2 Counter Status		R
0x200-0x21C	Timing Channel Mode Register	Timing Channel 6	R/W
0x220	Phase 1 Cycle Part 1 Register		R/W
0x224	Phase 1 Cycle Part 2 Register		R/W
0x228	Phase 2 Cycle Part 1 Register		R/W
0x22C	Phase 2 Cycle Part 2 Register		R/W
0x230	Phase 2 Delay Register		R/W
0x234	Phase 2 Duration Register		R/W
0x238	Phase 1 Counter Status		R
0x23C	Phase 2 Counter Status		R
0x240-0x25C	Timing Channel Mode Register	Timing Channel 7	R/W
0x260	Phase 1 Cycle Part 1 Register		R/W
0x264	Phase 1 Cycle Part 2 Register		R/W
0x268	Phase 2 Cycle Part 1 Register		R/W
0x26C	Phase 2 Cycle Part 2 Register		R/W
0x270	Phase 2 Delay Register		R/W
0x274	Phase 2 Duration Register		R/W
0x278	Phase 1 Counter Status		R
0x27C	Phase 2 Counter Status		R
0x280-0x29C	Timing Channel Mode Register	Timing Channel 6	R/W
0x2A0	Phase 1 Cycle Part 1 Register		R/W
0x2A4	Phase 1 Cycle Part 2 Register		R/W
0x2A8	Phase 2 Cycle Part 1 Register		R/W
0x2AC	Phase 2 Cycle Part 2 Register		R/W
0x2B0	Phase 2 Delay Register		R/W
0x2B4	Phase 2 Duration Register		R/W
0x2B8	Phase 1 Counter Status		R
0x2BC	Phase 2 Counter Status		R
0x2C0-0x2FC	Timing Channel Status Register 1		R
0x300-0x3FC	Timing Channel Status Register 2		R

Higher addresses contain the same registers because only the least significant 10 address lines are used.
Because the registers are always addressed as 32 bits registers the least significant 2 address lines are not monitored.

2.1.1 General Control Register (0x000)

Bit	Description	R/W	Reset
3:0	**COMMAND**; Command given to the DIO2 to specify its operation. See also the **BUSY** bit in the General Status Register.	R/CW	0
11:4	**OPERANT**; Extra parameter used with **COMMAND**.	R/CW	0
12	**IOERRCLR**; Clears the I/O error status. This means clearing the I/O error status bits, enabling front outputs and changing the LED status from red to yellow/orange.	R/CW	0
13	**INTCLR**; Remove the generated PCI interrupt.	R/CW	0
31:14	Reserved	R	0

The following values are valid commands, which can be assigned to the **COMMAND** parameter.

COMMAND	Description	Valid in TCSTATUS
0000 (0x0)	Has no function	All
1110 (0xE)	**DISARM**; Disarm one or more timing channels. The selected timing channels are placed in the IDLE state immediately. The channel selection (1 to 8) must be entered in the **OPERANT** parameter.	ARMED, PHASE1, PHASE2
0001 (0x1)	**ARM**; Arm one or more timing channels so they are ready to receive triggers. The scalers/counters are not started in any situation (see START command). The channel selection (1 to 8) must be entered in the **OPERANT** parameter.	IDLE
0010 (0x2)	**START**; Start the selected timing channels. This can be used when, for a channel no start event has been defined. The timing channel goes to the PHASE1 state. The channel selection (1 to 8) must be entered in the **OPERANT** parameter.	ARMED
1101 (0xD)	**STOP**; Stop the selected timing channels. This can be used when, for a channel no stop event has been defined. The timing channel goes back to the ARMED state. The channel selection (1 to 8) must be entered in the **OPERANT** parameter.	PHASE1, PHASE2
0011 (0x3)	**TRIG**; Generate a software trigger for one or more timing channels. The channel selection (1 to 8) must be entered in the **OPERANT** parameter.	ARMED, PHASE1, PHASE2
1010 (0xA)	**GATEOFF**; Make the Timing channel gate signal inactive for one or more timing channels. The channel selection (1 to 8) must be entered in the **OPERANT** parameter.	IDLE, ARMED, PHASE1, PHASE2
1011 (0xB)	**GATEON**; Make the Timing channel gate signal active for one or more timing channels. The channel selection (1 to 8) must be entered in the **OPERANT** parameter.	IDLE, ARMED, PHASE1, PHASE2
1111 (0xF)	**EVENT**; generate a timing event. The timing event number must be entered in the **OPERANT** parameter (the most significant bit of **OPERANT** is ignored). Al least one Event Code Register must be configured as output to enable the optical transmission. When all Event Code Register are configured as input the use of event only affects this module.	IDLE, ARMED, PHASE1, PHASE2
0100 (0x4)	**STOPREC**; Stop recording timing events.	All
0101 (0x5)	**ARMREC**; Arm the timing event recorder so it can start recording timing events after receiving a recorder start timing event.	All
0111 (0x7)	**FLUSHREC**; Remove all recorded timing events.	All

For the commands TRIG, START, STOP, GATEON and GATEOFF the **OPERANT** parameter must be used for the channel selection. The least significant bit of **OPERANT** indicates timing channel 1 and the most significant bit indicates timing channel 8. So every individual timing channel can be accessed one at a time, all at once or just a selection.

2.1.2 General Status Register (0x004)

Bit	Description	R/W	Reset
0	**BUSY**; A command entered in the General Control Register is being processed. Further commands are ignored when **BUSY** is set. Because the timing channels are working at a different clock rate than the CompactPCI (local bus) side the entered command has to be synchronized which takes some time during which new commands can not be entered. **BUSY** is active for a maximum time of 200ns.	R	0
1	**TCINTEVENT**; PCI interrupt event has been generated after receiving a trigger, which affected one of the timing channel. Which timing channel has caused the interrupt can be found in the Timing Channel Status Register 1.	R	0
2	**RECINTEVENT**; PCI interrupt event has been generated because the event recorder FIFO is half full.	R	0
3	**IOERRINTEVENT**; PCI interrupt event has been generated because a front I/O error has occurred.	R	0
7:4	Reserved	R	0
8	**OPTOPARERR**; Parity error on the received timing highway event code.	R	0
15:9	Reserved	R	0
31:16	**IOERR**; A short circuit has been detected on one or more of the two front panel I/O connectors. The least significant bit of IOERR indicates an error on I/O channel 1, the most significant bit on channel 16.	R	0

2.1.3 Clock Control Register (0x008)

Bit	Description	R/W	Reset
1:0	**CLKSRC**; The selection of the timing channel clock source. 00 = Internal Clock 01 = Front/Rear I/O external clock 10 = PXI_TRIG7 11 = Timing Highway	R/W	00
5:2	**CLKCH**; Selection of the channel when **CLKSRC** is set to the values 10 (= external clock). 0x0 is channel 1 (front or rear) and 0xF is channel 16 (front or rear).	R/W	0
6	**CLKEDGE**; Selection of the active clock edge of the clock source. 0 = Rising edge. 1 = Falling edge.	R/W	0
7	**CLKOK**; The selected clock is present. When this bit is cleared the clock is not present or active, or the clock frequency is below 150kHz.	R	0
8	**CLKTHSYNC**; Synchronize the (re)generated Timing highway clock/data output signal to the received Timing highway input signal. The delay between the received clock and regenerated clock will be about 100ns. The jitter will be 25ns maximum.	R/W	0
9	**CLKTHOUT**; Enable the Timing highway output even when only Event decoders (see Event Code Registers) are used. When encoders are used, this parameter has no effect.	R/W	0
31:8	Reserved	R	0

CLKSRC	IOCH	Description
00	XXXX	Internal Clock
01	0000 – 1111	Front/Rear panel digital I/O channel 1 to 16
10	XXXX	PXI Trigger input signal PXI_TRIG7
11	0000 – 0111	Timing channel 1 to 8
11	1000 – 1111	Timing channel 1 to 8

Note: During and after the change of the timing channel clock source the parts of the design, which use this clock, will be resetted. This will also cause the **CLKOK** bit to be cleared until this reset is inactive again and a clock edge had been detected. When the Timing Highway is used as clock source the derived clock will be synchronized to the Timing Highway clock during this reset period. When the Timing Highway clock is not present during this clock source selection there could be a clock skew of 75ns (max) between DIO2s.

Note: When PXI_TRIG7 or the Front/Rear I/O external clock is used these clocks must be four times the desired frequency. So for example with a timing channel clock of 10MHz, PXI_TRIG7 must run at 40MHz. The maximum allowable frequency of PXI_TRIG7 is 40MHz. The Rear I/O clock maximum is 20MHz, and the maximum allowable frequency of the Front I/O clock is 10MHz. This would result in a timing channel clock of 5MHz max.

2.1.4 Version and Reset Register (0x00C)

Bit	Description	R/W	Reset
7:0	**REVISION**; ASCII character '0'	R	0x30
15:8	**VERSION**; ASCII character 'A'	R	0x41
23:16	**2**; ASCII character '2'	R	0x32
31:24	**DIO**; ASCII character 'D'	R	0x44

Bit	Description	R/W	Reset
0	**RESET**; When this bit is set the DIO2 will be resetted locally. FIFOs and memories are flushed and all parameters are cleared.	CW	n.a
31:1	Reserved	W	n.a

2.1.5 I/O Connection Registers, channel 1 to 16 (0x010-04C)

Bit	Description	R/W	Reset
0	**IODIR**; Selection of the direction between input and output. 0 = Input 1 = Output When the **IODIR** is set to 'Output' all 'Input' features will remain functional and available.	R/W	0
1	**IOSIDE**; Which I/O side is used. 0 = Front: Input comes from front and output goes to front digital I/O. 1 = Rear: Input comes from rear and output goes to rear digital I/O.	R/W	0
3:2	**IOSRC**; Source of the output signal. 00 = Register: Writing to the I/O register will affect the output. 01 = Buffer: Copy the signal of a front or rear input. 10 = PXI trigger input. The PXI trigger input signal is buffered to the Front or Rear output, dependant on **IOSIDE**. 11 = Timing channel.	R/W	0
7:4	**IOCH**; Selection of the channel when **IOSRC** is not set to 00 (= Register).	R/W	0
8	**IO50OHM**; Select the 50Ω input termination for the front input. This bit is only functional when the front I/O is set to Input. However it can be used with all settings of **IODIR** and **IOSIDE**, but is ignored when the front side output is used since input termination on an output is illegal.	R/W	0
9	**IOERRINTEN**; Enable PCI interrupt generation after detecting a front I/O error on this I/O channel.	R/W	0
31:10	Reserved	R	0

IOSRC	IOCH	Description
00	XXXX	Register to output
01	0000 – 1111	Front/Rear panel digital I/O channel 1 to 16
10	0000 – 0111	PXI Trigger input signals PXI_TRIG0 to PXI_TRIG7
10	1000 – 1111	PXI Trigger input signals PXI_TRIG0 to PXI_TRIG7
11	0000 – 0111	Timing channel 1 to 8
11	1000 – 1111	Timing channel 1 to 8

2.1.6 PXI Connection Registers, trigger 0 to 7 (0x050-0x06C)

Bit	Description	R/W	Reset
0	**PXIDIR**; Selection of the direction between input and output. 0 = Input 1 = Output When the direction is set to 'Output' all 'Input' features will remain functional and available.	R/W	0
2:1	**PXISRC**; Source of the output signal. 00 = Register: Writing to the I/O register will affect the output. 01 = Buffer: Copy the signal of a front or rear input. 10 = Reserved 11 = Timing channel.	R/W	0
6:3	**PXICH**; Selection of the channel when **PXISRC** is not set to 00 (= Register).	R/W	0
31:7	Reserved	R	0

PXISRC	PXICH	Description
00	XXXX	Register to output
01	0000 – 1111	Front/Rear panel digital I/O channel 1 to 16
10	XXXX	Reserved
11	0000 – 0111	Timing channel 1 to 8
11	1000 – 1111	Timing channel 1 to 8

2.1.7 I/O Register (0x070)

Bit	Description	R/W	Reset
15:0	**IO**; When writing to **IO** the Front or Rear outputs are changed when they are configured as output and their source is the I/O register. When reading, the input value from the Front or Rear is read, depending on **IOSIDE**.	R/W	0
23:16	**PXIIO**; When writing to **PXIIO** the PXI outputs are changed when they are configured as output and their source is the I/O register. When reading, the input value from the PXI trigger inputs is read.	R/W	0
31:24	Reserved	R	0

2.1.8 Event Recorder Register (0x074)

Bit	Description	R/W	Reset
6:0	**EREVENT**; Timing event code, which starts the recording of all further received timing events.	R/W	0
8:7	**ERSTATUS**; The timing event recorder current status. 00 = Idle (stopped). 01 = Armed. 10 = Recording. 11 = Paused because FIFO is full. See General Control Register for Event Recorder specific commands.	R	0
14:9	**ERCOUNT**; Counts number of recorded events. The maximum is 32. ERCOUNT is decreased after reading the Event Recorder Code Register.	R	0
15	**ERINTEN**; Enable PCI interrupt generation when the event recorder FIFO is half full.	R/W	0
31:16	Reserved	R	0

2.1.9 Event Recorder Code Register (0x078)

Bit	Description	R/W	Reset
6:0	**ERCODE**; Recorded event code. This parameter is the interface to a FIFO, which contains a total of **ERCOUNT** recorded event codes. **ERCODE** belongs to the **ERTIME** in the Event Recorder Time Register, so must be read together with **ERCODE** When **ERCOUNT** equals 0 the value of **ERCODE** is invalid.	R	0
31:7	Reserved	R	0

2.1.10 Event Recorder Time Register (0x07C)

Bit	Description	R/W	Reset
31:0	**ERTIME**; Number of counted clock cycles since received start timing event code **EREVENT**. At which an event has been recorded. This parameter is the interface to a FIFO, which contains a total of **ERCOUNT** recorded event code times. **ERTIME** belongs to the **ERCODE** in the Event Recorder Code Register, so must be read together with **ERCODE**. When **ERCOUNT** equals 0 the value of **ERTIME** is invalid.	R	0

2.1.11 Event Code Registers, 1 to 16 (0x080-0x0BC)

Bit	Description	R/W	Reset
6:0	**ECEVENT**; Timing event code, which should be recognized and used. Event code 0x00 will be ignored when received from the timing highway, so will not have effect on the event code recognition. However when event code 0x00 is given using an EVENT command the event code is recognized. Event code 0x00 can be transmitted over the timing highway when **ECDIR** is set to transmit.	R/W	0
14:7	**ECCHEN**; Timing channel enable. The channels (1 to 8), which must receive a timing event trigger after receiving the timing event specified in **ECEVENT**. The least significant bit of **ECCHEN** indicates timing channel 1 and the most significant bit indicates timing channel 8. *This parameter only applies to the Event Code Receive mode.*	R/W	0
16:15	**ECTIMEEV**; Trigger (Timing Event) type sent to the timing channel counters after receiving the specified event code. 00 = General purpose timing event trigger. 01 = Start timing event trigger. When the timer channel is already started this event is not used. 10 = Stop timing event trigger. When the timer channel is not started this event is not used. 11 = Reserved *This parameter only applies to the Event Code Receive mode.*	R/W	0
17	**ECDIR**; Selection of the event code use. 0 = Receive (Decode). Use **ECEVENT** to trigger timing channels. 1 = Transmit (Encode) the **ECEVENT** event code after receiving a trigger. **ECCHEN**, **ECSTART** and **ECSTOP** are ignored.	R/W	0
18	**ECTRIGEDGE**; Selection of the active edge of the trigger signal 0 = Rising edge. 1 = Falling edge. *This parameter only applies to the Event Code Transmit mode.*	R/W	0
20:19	**ECTRIGSRC**; Source of the trigger when ECDIR is set to Transmit. The event code is transmitted after receiving a trigger on one of the following signals. 00 = PXI star trigger input. 01 = Front/Rear: Use the signal of a front or rear input. 10 = PXI trigger input. 11 = Reserved *This parameter only applies to the Event Code Transmit mode.*	R/W	0
24:21	**ECTRIGCH**; Selection of the channel when **ECTRIGSRC** is not set to 00 (= PXI start trigger input). When **ECTRIGSRC** is set to 10 (=PXI trigger input) the most significant bit of **ECGATECH** is ignored. *This parameter only applies to the Event Code Transmit mode.*	R/W	0
31:25	Reserved	R	0

When both **ECSTART** and **ECSTOP** are selected the two bits are cleared and the timing event remains active as a non-explicit start or stop timing event.

ECTRIGSRC	ECTRIGCH	Description
00	XXXX	PXI star trigger input
01	0000 – 1111	Front panel digital I/O channel 1 to 16
10	0000 – 0111	PXI trigger input 0 to 7
10	1000 – 1111	PXI trigger input 0 to 7
11	XXXX	Reserved

Note: Transmit is enabled using **ECDIR**. Receive is enabled through **ECCHEN**.

2.1.12 Timing Channel Mode Registers, channel 1 to 8

Bit	Description	R/W	Reset
1:0	**TCTRIG**; Selection of the external source of the trigger signal 00 = Trigger disabled 01 = I/O trigger (rising edge). Through Front, Rear or PXI. 10 = I/O trigger (falling edge). Through Front, Rear or PXI. 11 = Timing event. Through optical input or software command. A software TRIG command remains always available.	R/W	0
3:2	**TCTRIGSRC**; Source of the trigger when TCTRIG is an I/O trigger (001 or 010). 00 = PXI star trigger input. 01 = Front/Rear: Use the signal of a front or rear input. 10 = PXI trigger input. 11 = Reserved	R/W	0
7:4	**TCTRIGCH**; Selection of the channel when **TCTRIGSRC** is not set to 00 (= PXI start trigger input). When **TCTRIGSRC** is set to 10 (=PXI trigger input) the most significant bit of **TCGATECH** is ignored.	R/W	0
9:8	**TCGATE**; Selection of the external source of the gate signal 00 = Gate disabled 01 = I/O gate (low level). Through Front, Rear or PXI. 10 = I/O gate (high level). Through Front, Rear or PXI. 11 = Reserved. A software GATEON or GATEOFF command remains always available. Since the external gate source is OR-ed with the GATEON/GATEOFF command the timing channel must be placed in the GATEOFF mode to enable the use of the external gate.	R/W	0
11:10	**TCGATESRC**; Source of the gate when TCGATE is an I/O gate (01 or 10). 00 = PXI star trigger input. 01 = Front/Rear: Use the signal of a front or rear input. 10 = PXI trigger input. 11 = Reserved	R/W	0
15:12	**TCGATECH**; Selection of the channel when **TCGATESRC** is not set to 00 (= PXI start trigger input). When **TCGATESRC** is set to 10 (=PXI trigger input) the most significant bit of **TCGATECH** is ignored.	R/W	0
16	**TCGATESYNC**; When set the gate signal is synchronized to the end of a cycle part. So to the end of part 1 or 2 of a cycle in phase 1 or 2. 0 = Asynchronous gate 1 = Synchronous gate	R/W	0
17	**TCCYCLIC**; When set, indicates that the channel is ready to receive a new trigger with is has switched back to Phase 1.	R/W	0
18	**TCTERM2**; When set, terminates Phase 2 after receiving a trigger. When this bit is set the Phase 2 Duration Register value is not used.	R/W	0
19	**TCIDLELEV**; The default output level of the timing channel when the DIO2 is disarmed (IDLE) or when the output during phase 1 or 2 is not driven by one of the cycle part counters.	R/W	0
20	**TCINTEN**; Enable PCI interrupt generation after receiving a trigger, which affected the timing channel.	R/W	0
21	**PH1CYC1LEV**; The phase 1 starting level. The output level of cycle part 1 of phase 1. This is the output level with which phase 1 output starts. Default this is high and so the next level of the output will be low. With this it is possible to select an inverted or non-inverted signal.	R/W	1
22	**PH1CYC2LEV**; The level of phase 1, cycle part 2. This is the output level of the last part of a clock cycle generated within phase 1.	R/W	0
23	**PH2CYC1LEV**; The phase 2 starting level. The output level of cycle part 1 of phase 2. This is the output level with which phase 2 output starts.	R/W	1
24	**PH2CYC2LEV**; The level of phase 2, cycle part 2. This is the output level of the last part of a clock cycle generated within phase 2.	R/W	0
31:25	Reserved	R	0

TCTRIGSRC / TCGATESRC	TCTRIGCH	Description
00	XXXX	PXI star trigger input
01	0000 – 1111	Front panel digital I/O channel 1 to 16
10	0000 – 0111	PXI trigger input 0 to 7
10	1000 – 1111	PXI trigger input 0 to 7
11	XXXX	Reserved

Note: Changing the contents of the Timing Channel Mode Register can only be done when the timing channel is in the **IDLE** state.

2.1.13 Phase 1 Cycle Part 1 Registers, channel 1 to 8

Bit	Description	R/W	Reset
31:0	**PH1CYCLE1**; The number of counted clock cycles + 1, which the first part of an output cycle in phase 1, must last. The output level is defined with **PH1CYC1LEV**. *This register will not be cleared after a reset (Reset Register).*	R/W	X

2.1.14 Phase 1 Cycle Part 2 Registers, channel 1 to 8

Bit	Description	R/W	Reset
31:0	**PH1CYCLE2**; The number of counted clock cycles + 1, which the second part of an output cycle in phase 1, must last. The output level is defined with **PH1CYC2LEV**. *This register will not be cleared after a reset (Reset Register).*	R/W	X

2.1.15 Phase 2 Cycle Part 1 Registers, channel 1 to 8

Bit	Description	R/W	Reset
31:0	**PH2CYCLE1**; The number of counted clock cycles + 1, which the first part of an output cycle in phase 2, must last. The output level is defined with **PH2CYC1LEV**. *This register will not be cleared after a reset (Reset Register).*	R/W	X

2.1.16 Phase 2 Cycle Part 2 Registers, channel 1 to 8

Bit	Description	R/W	Reset
31:0	**PH2CYCLE2**; The number of counted clock cycles + 1, which the second part of an output cycle in phase 2, must last. The output level is defined with **PH2CYC2LEV**. *This register will not be cleared after a reset (Reset Register).*	R/W	X

2.1.17 Phase 2 Delay Registers, channel 1 to 8

Bit	Description	R/W	Reset
31:0	**PH2DELAY**; The number of counted clock cycles + 1, which the delay between the trigger recognition and the switch from phase 1 to phase 2 must last. The output remains working in phase 1 until the switch over. *This register will not be cleared after a reset (Reset Register).*	R/W	X

2.1.18 Phase 2 Duration Registers, channel 1 to 8

Bit	Description	R/W	Reset
31:0	**PH2DUR**; The number of counted clock cycles + 1, which phase 2 lasts until it is automatically terminated. Only used when **TCTERM2** is not set. *This register will not be cleared after a reset (Reset Register).*	R/W	X

2.1.19 Phase 1 Counter Status Registers, channel 1 to 8

Bit	Description	R/W	Reset
31:0	**PH1COUNT**; The number of counted timing channel clock cycles which phase 1 is currently active or lasted. The counter is cleared when the timing channel is armed. The counter value starts (at 0) when the timing channel is started, and stops when the timing channel has switched to phase 2. The counter will not continue when the timing channel switches back to phase 1. So only the first phase 1, after arming the timing channel, will be counted. *This register will not be cleared after a reset (Reset Register).* *It will be cleared when the timing channel is in the Armed state.*	R	X

2.1.20 Phase 2 Counter Status Registers, channel 1 to 8

Bit	Description	R/W	Reset
31:0	**PH2COUNT**; The number of counted timing channel clock cycles which phase 2 is currently active or lasted. The counter is cleared when the timing channel is armed. It starts counting when phase 2 has been entered and stops when phase 2 terminates. Only the first phase 2, after arming the timing channel, will be counted. *This register will not be cleared after a reset (Reset Register),* *It will be cleared when the timing channel is in the Armed state.*	R	X

2.1.21 Timing Channel Status Register 1 (0x2C0-2FC)

Bit	Description	R/W	Reset
7:0	**TCLEVEL**; The timing channel's current output level. The least significant bit of **TCLEVEL** indicates the current level for timing channel 1. The most significant bit indicates the current output level for timing channel 8.	R	0
15:8	**TCTRIGGERED**; These bits are set when the timing channel has been triggered. These bits are cleared when the DIO2 is Disarmed.	R	0
23:16	**TCINT**; PCI interrupt event has been generated after receiving a trigger, which affected the timing channel. The least significant bit of **TCINT** indicates an interrupt for timing channel 1. The most significant bit indicates an interrupt for timing channel 8.	R	0
31:24	Reserved	R	0

2.1.22 Timing Channel Status Register 2 (0x300-3FC)

Bit	Description	R/W	Reset
1:0	**TCSTATUS1**; The timing channel 1 current status.	R	0
3:2	**TCSTATUS2**; The timing channel 2 current status.	R	0
5:4	**TCSTATUS3**; The timing channel 3 current status.	R	0
7:6	**TCSTATUS4**; The timing channel 4 current status.	R	0
9:8	**TCSTATUS5**; The timing channel 5 current status.	R	0
11:10	**TCSTATUS6**; The timing channel 6 current status.	R	0
13:12	**TCSTATUS7**; The timing channel 7 current status.	R	0
15:14	**TCSTATUS8**; The timing channel 8 current status.	R	0
31:16	Reserved	R	0

TCSTATUSx	Description
00	**IDLE**; The timing channel is doing nothing. It has been DISARMed.
01	**ARMED**; The timing channel has been ARMed and is waiting for a start trigger/event or START command.
10	**PHASE1**; The timing channel is active in phase 1.
11	**PHASE2**; The timing channel is active in phase 2.

2.2 CompactPCI interface

2.2.1 Mechanical

The CompactPCI interface is provided using the standard Hard Metric 2mm type A connector. This connector (J1) is available at the rear side of the board.

2.2.2 Electrical

The CompactPCI interface is implemented using a PLX PCI9054 PCI Controller. This controller is compliant to the “PCI Local Bus Specification, Revision 2.2”.

• DC Power	5 Volt and 3.3 Volt through J1

2.2.3 Functional

The CompactPCI interface is implemented compliant to “PCI Local Bus Specification, Revision 2.2” and “PICMG 2.0 R3.0 CompactPCI Specification”.
The interface has the following features and characteristics.

• Bus width	32 bit
• Clock	33 MHz
• Configuration	Target (Slave)
• Interrupt	INTA# generated on: • Timing channel received trigger • Event Recorder FIFO half full • Front I/O error detection
• Hot swap	No
• Geographical addressing	No

2.2.4 Allocation

The CompactPCI interface is completely implemented through connector J1.
CompactPCI specific signals through J2 are not used.

2.3 PXI interface

2.3.1 Mechanical

The PXI interface is provided using the standard Hard Metric 2mm type B connector. This connector (J2) is available at the rear side of the board.

2.3.2 Electrical

The PXI interface is implemented compliant to the “PXI Specification, Revision 2.0”

2.3.3 Functional

The PXI interface is implemented compliant to “PXI Specification, Revision 2.0”. Not all features of the PXI standard are available. Only the following can be used.

- Trigger input: PXI Star Trigger (**PXI_STAR**) and the PXI Trigger bus signals (**PXI_TRIG[7:0]**).
- Timing output: The PXI Trigger bus signals (**PXI_TRIG[7:0]**).
- Clock output: The most significant PXI Trigger bus signals (**PXI_TRIG7**). This output is capable if creating a clean clock signal.

When **PXI_TRIG7** is used for the timing channel clock generation (See Clock Control Register) the frequency must not exceed 40MHz.

The trigger signals cannot be synchronized to the **PXI_CLK10**. The **PXI_CLK10** signal is not used.

2.3.4 Allocation

The PXI interface is implemented through connector J2. CompactPCI specific signals through J2 are not used.

2.4 Front panel digital in/out

2.4.1 Mechanical

The I/O interfaces are provided using 16 coaxial (uni-pole) connectors, type EPL.00.250.NTN from LEMO. These connectors are available through the front panel.

2.4.2 Electrical

The I/O interface can be configured as **INPUT** or **OUTPUT**. When the output is not used the input can have a selectable line termination of 50Ω. The output is capable of driving a 50Ω cable with termination.

Input characteristics

• High-level input voltage (min)	2V
• Low-level input voltage (max)	0.8V
• Input voltage	-2V (clamped at -0.3) to 7V
• Input threshold level	± 1.4V with 0.4V hysteresis
• Input impedance	± 5kΩ
• Line termination	50Ω (selectable)

Output characteristics

• High-level output voltage (min)	4.8V (no line termination) 2.4V (with 50Ω line termination)
• Low-level output voltage (max)	0.4V
• Output current	50mA (with 50Ω line termination)
• Output short-circuit current	140mA (max)
• Short-circuit duration	Continuous
• Short-circuit to voltage level	-2V to 7V

Note: The output is always read back through the input. When the input signal level (high or low) is not equal to the driven output signal level, the output will be put in a high impedance state. A front panel LED and a status bit indicate this. An interrupt can be generated.

Note: This I/O error detection works up to a driving frequency of above 5MHz (the maximum Timing Channel output frequency), when short circuited to 0V. Output signals with a frequency above 5 to 7MHz will not trigger the short circuit detection. When a short circuit is made to another voltage level than 0V, the I/O error detection can work up to a

frequency below 5MHz. This frequency depends on parameters like the short circuit voltage level, the maximum current drive and output resistance of the short circuiting output driver.

2.4.3 Functional

The I/O interface can have different logical functions, which are defined in the FPGA of the DIO2.
As stated before, the output is monitored through the input to detect possible short circuit situations. When such a situation has been detected the output is placed in it's high impedance state until the problem has been resolved and this I/O error is cleared. Clearing the I/O error can be done through a CompactPCI addressable register.

When a front I/O is used for the timing channel clock generation (See Clock Control Register) the frequency must not exceed 10MHz.

2.4.4 Allocation

The I/O interfaces can be accessed using a LEMO series 00 connector located in the front panel of the DIO2.
Next to each I/O interface connector there is a LED, which indicate the following statuses.

LED	In/Out	Status
Off	-	I/O disabled (Rear side selected), Power off or FPGA not configured
Green	In	Input selected (Green = Everything OK)
Yellow/Orange	Out	Output selected (Yellow = Attention, this is a output)
Red	In (Out in 3-State)	Short circuit detected (Red = Error)

2.5 Rear panel digital in/out

2.5.1 Mechanical

The Rear I/O interface is provided using the standard Hard Metric 2mm type B connector. This connector (J5) is available at the rear side of the board.

2.5.2 Electrical

The Rear I/O interface consists of several signals.
Provided are the CompactPCI +5V and +3.3V for use by the Transition module. These are power supply outputs.
The separate +5V power supply for the Optical I/O can be provided here. This is a power supply input.
The 16 digital rear I/O signals have the following characteristics:

Input characteristics

• High-level input voltage (min)	2V
• Low-level input voltage (max)	0.8V
• Input voltage	-0.5V to 5.5V
• Input clamp current	-50mA

Output characteristics

• High-level output voltage (min)	4.8V
• Low-level output voltage (max)	0.4V
• Output type	Open collector with 1kΩ pull-up to +5V.

Power characteristics

• DC Power	5 Volt through J5
• Current	70mA (typ)

2.5.3 Functional

The Rear I/O interface can have different logical functions, which are defined in the FPGA of the DIO2.

When a rear I/O is used for the timing channel clock generation (See Clock Control Register) the frequency must not exceed 20MHz.

2.5.4 Allocation

The Rear I/O is implemented so it does not become incompatible with the following standards.

- VITA 29.1(PC•MIP Pin Mapping to CompactPCI and VME64X)
- PICMG 2.3 (PMC I/O Pin Assignments on CompactPCI)
- PICMG 2.4 (IP I/O Pin Assignments on CompactPCI)

These standards could be used by different Transition Modules to interface with CompactPCI modules. In all three cases the Rear I/O signals and the Optical I/O power supply can be accessed as if there was a PC•MIP, PMC or IndustryPack module attached in the DIO2.

The interface is implemented through connector J5 only. For VITA 29.1 only the PC•MIP-U is available. For PICMG 2.3 only the I/O pins 1 to 55 are connected and defined. For PICMG 2.4 only Slot D is available.

Pin	Row A	Row B	Row C	Row D	Row E	Row F	Compliance		
22	**+3.3V**	**+3.3V**	**+3.3V**	**+5V**	**+5V**	GND		IndustryPack Slot D	PMC I/O 1 to 64
21	GND	GND	GND	**OPTO +5V**	**OPTO +5V**	GND	PC•MIP-U		
20	GND	GND	GND	**REAR 1**	**REAR 2**	GND			
19	GND	GND	GND	**REAR 3**	**REAR 4**	GND			
18	GND	GND	GND	**REAR 5**	**REAR 6**	GND			
17	GND	GND	GND	**REAR 6**	**REAR 8**	GND			
16	GND	GND	GND	**REAR 9**	**REAR 10**	GND			
15	GND	GND	GND	**REAR 11**	**REAR 12**	GND			
14	GND	GND	GND	**REAR 13**	**REAR 14**	GND			
13	GND	GND	GND	**REAR 15**	**REAR 16**	GND			
12	**+3.3V**	**+3.3V**	**+3.3V**	**+5V**	**+5V**	GND			
11	n.c.	n.c.	n.c.	n.c.	n.c.	GND			
10	n.c.	n.c.	n.c.	n.c.	n.c.	GND			
9	n.c.	n.c.	n.c.	n.c.	n.c.	GND			
:	n.c.	n.c.	n.c.	n.c.	n.c.	GND			
1	n.c.	n.c.	n.c.	n.c.	n.c.	GND			

Signal	Pin PC•MIP-U	Pin IndustryPack Slot D	Pin PMC I/O
REAR 1	11	14	12
REAR 2	12	15	11
REAR 3	17	19	17
REAR 4	19	20	16
REAR 5	24	24	22
REAR 6	25	25	21
REAR 7	31	29	27
REAR 8	32	30	26
REAR 9	38	34	32
REAR 10	39	35	31
REAR 11	44	39	37

Signal	Pin PC•MIP-U	Pin IndustryPack Slot D	Pin PMC I/O
REAR 12	46	40	36
REAR 13	51	44	42
REAR 14	52	45	41
REAR 15	57	49	47
REAR 16	59	50	46
+5V	63-64	4-5	1-2, 51-52
+3.3V	60-62	1-3	3-5, 53-55
OPTO +5V	4, 6	9-10	6-7
GND	1-3, 7-9, 14-16, 20, 22-23, 27-28, 30, 33, 35-36, 40-41, 43, 47-49, 54-56	6-8, 11-13, 16-18, 21-23, 26-28, 31-33, 36-38, 41-43, 46-48	8-10, 13-15, 18-20, 23-25, 28-30, 33-35, 38-40, 43-45, 48-50
n.c.			56-64

2.6 Optical In/Out

2.6.1 Mechanical

The Optical I/O interface is provided using two ST optical connectors. These connectors are available through the front panel.

2.6.2 Optical/Electrical

The Optical I/O interface has one **INPUT** and one **OUTPUT**. The input is implemented using an HFPR-2416 Optical Receiver, and the output is implemented using an HFPR-1414 Optical Transmitter, both from Agilent. For detailed characteristics see the datasheets of these devices.
Both devices operate best with light with a wave length of 820nm, using a 62.5/125 mm multimode glass fiber cable.

2.6.3 Logical

The Optical I/O interface can be used in different modes.

- The optical input can be used as the source for the Timing Highway.
- The optical output can have it's source from the optical input directly. This can be selected during operational mode or is automatically selected when the CompactPCI power is turned off. This automatic bypass mode is only available when a separate power supply (+5V) is provided through J5.
- The optical output can also be a signal generated from within the FPGA.

2.6.4 Allocation

The Optical I/O interfaces can be accessed using two ST connectors. These two connectors will be available through the front panel and located at the top of the front panel.

2.7 LED User Interface

2.7.1 Function

There are two groups of LEDs to give information to the user. The first group consists of the three color LEDs which indicate the I/O status of the front panel digital I/Os.

I/O Status LED	Digital In/Out	Status
Off	-	I/O disabled (Rear side selected), Power off or FPGA not configured
Green	In	Input selected (Green = Everything OK)
Yellow/Orange	Out	Output selected (Yellow = Attention, this is a output)
Red	In (Out in 3-State)	Short circuit detected (Red = Error)

The other group of LEDs are used to indicate the functional mode of the DIO2. All three LEDs are yellow.

Function LED	Description
Clock OK	Optical clock is present
Event	Event has been received
Backup +5V OK	OPTO +5V backup power is present

2.7.2 Allocation

The I/O status LEDs are located in the front panel, next to the LEMO connectors. One next to each front panel digital I/O interface.
The function LEDs are also located in the front panel, at the top of the front panel.

3 ALLOCATION