NCSX June 2007 ETC
TABLE I - DESIGN LABOR

WBS Number: 54

WBS Title: Facility Timing & Synchronization Systems

Job Number: 5401

Job Title: Data Acquistion & Facility Computing Systems

Job Manager: Paul Sichta

Description:

Title I and ...

		FY07$K											
Activity ID	**Activity Description**	**41MS**	**43MS/CC**	**48MS**	**37STK**	**35TRVL**	ECEM	ECTB	EMTB	EASB	EEEM	EETB	**Basis of Estimate**
													Originally manhours estimate based on NSTX experience. However, this estimate has been updated to reflect experience of experieince on other similar networking installation projects.
54-10	Preliminary System Design						40						
54-20	Final SystemDesign						40						
54-30	Preliminary Design - Clock Dist.						20				40		
54-40	Final Design - Clock Dist.						20				120		
54-50	Test - Clock Dist.						20				100	120	
54-60	Procurement	$16K	$14K		$4K		40						
54-70	UNT - Timing & Seq Emulation (FPGA Pgm)							160					
54-80	UNT - Device Driver Prog (EPICS/MDSplus)						160						
54-90	Central Clock (EPICS) Programming						80						
54-100	Installation						40	80	120	40			
54-110	Test						40	40					
	Subtotal Job 5401	***$16K***	***$14K***	***$0K***	***$4K***	***$0K***	***500***	***280***	***120***	***40***	***260***	***120***	