

NCSX PRELIMINARY DESIGN PART I - DESCRIPTION

<b>WBS Number: 54</b>	<b>Title: NCSX Facility Timing and Synchronization</b>
<b>Originator: G. E. Oliaro</b>	
<p><b><u>Description</u></b></p> <p><u>General Description of Work to be Performed:</u> A new timing and synchronization technology is required for NCSX. The old CAMAC based TFTR Timing System, developed in the late 70's, with only a 1MHz time base will not be adequate for NCSX. A requirement for a 10 MHz time base and an off-the-shelf or existing solution for NCSX is highly desirable. An internally developed Field Programmable Gate Array (FPGA) PCI design running at 10MHz will be deployed for NCSX. We will have two years of operational experience on NSTX with this system and will use the existing design for NCSX.</p> <p>Specifications: * Timing granularity of ~100ns * Overall accuracy +/- 1us with contention * 128 or greater event triggers * Fiber optic broadcast transmission</p> <p>This activity will provide the engineering design and test of a PCI clock encoder module and manpower to write driver software.</p> <p><u>Description of Existing Equipment/Facilities to be Reused:</u> No existing equipment will be used. - - - - - - -</p> <p><u>Description of Major Modifications Required to Existing Equipment/Facilities:</u> No modifications to existing equipment will be required. - -</p>	